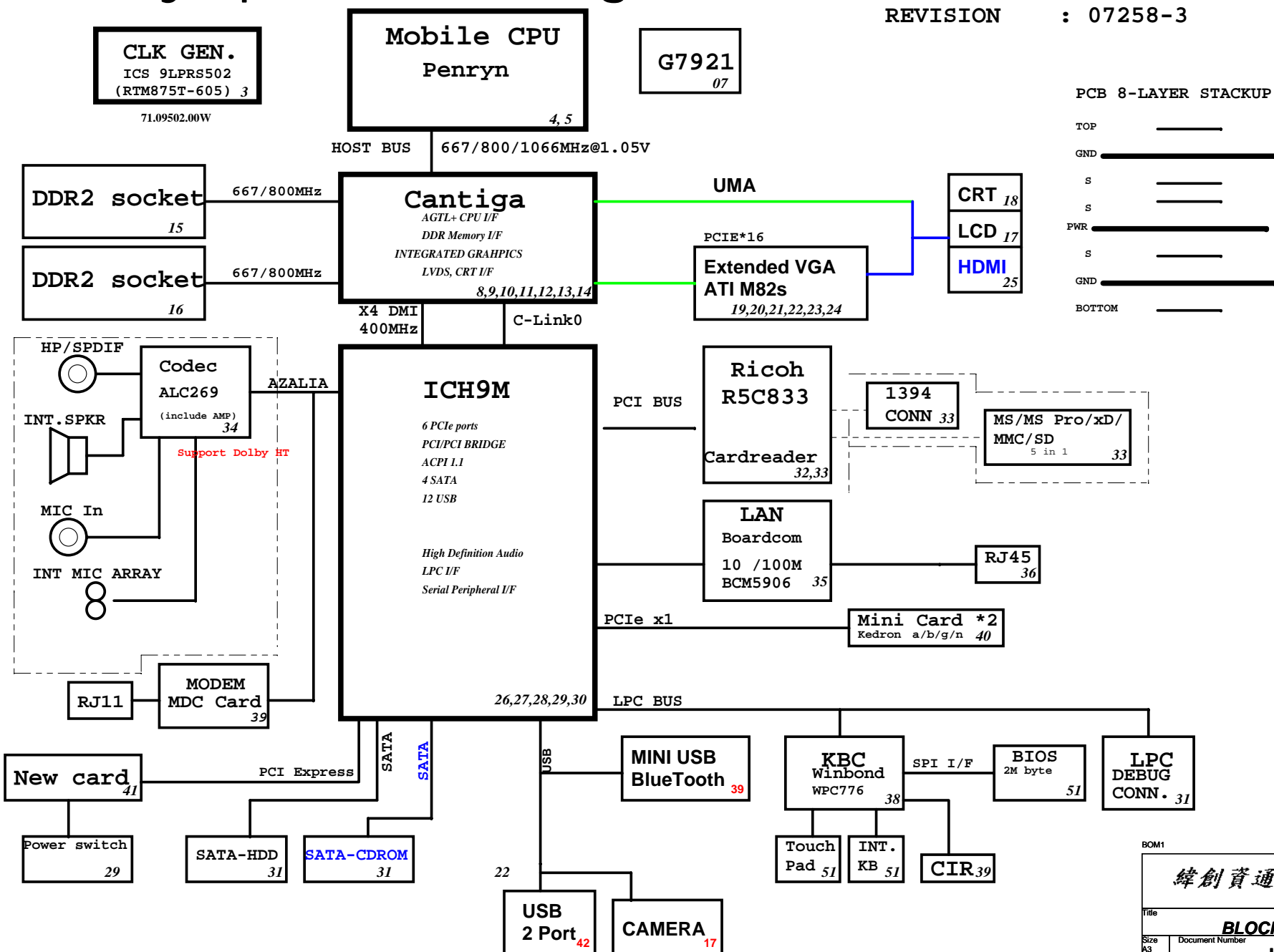


Olympus Block Diagram

Project code: 91.4Y601.001
PCB P/N : 48.4Y603.0SA
REVISION : 07258-3



SYSTEM DC/DC ISL6236 38	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(5A) 3D3V_S5(5A)
SYSTEM DC/DC TPS51124 40	
INPUTS	OUTPUTS
DCBATOUT	1D05V_M(11A) 1D5V_S3(10A)
TPS51117 39	
DCBATOUT	1D8V_S3 (2.5A)
TPS51100 39	
1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3
APL5308 39	
3D3V_S0	2D5V_S0 (300mA)
CHARGER BQ24750 42	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA
CPU DC/DC ISL6266A 37	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A
NB DC/DC ISL6263A 41	
INPUTS	OUTPUTS
DCBATOUT	GFX_CORE
SC411 48	
DCBATOUT	1D5V_S3

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
BLOCK DIAGRAM			
Size A3	Document Number LT32M		Rev -3
Date: Monday, July 07, 2008	Sheet 1 of 55		

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers: Offset 224h).
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers: Offset 0224h).
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override, Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1, Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h; bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal, Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLFVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/ GPIO58/ CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

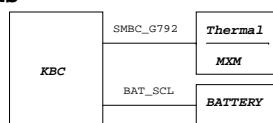
Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5
Page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB867 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) 1 = The iTPM Host Interface is disabled (default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes, 15->0, 14->1 ect.. 1 = Normal operation (Default): Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1 = Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALL mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH -> ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH -> ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default). 1 = Digital display Port and PCIE are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

SMBus



USB Table

Pair	Device
0	Combo (ESATA/USB)
1	NC
2	USB2
3	USB4
4	USB3
5	BLUETOOTH
6	WEBCAM
7	FT
8	MINICARD
9	NEW1

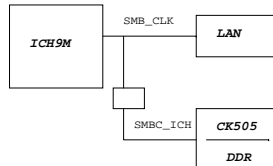
PCI Routing

page 17

IDSEL	INT	REQ	GNT
TI7412	AD22	G: CARDBUS B: 1394 F: Flash Media S: SD Host	0 0

PCIE Routing

LANE2	MiniCard WLAN
LANE3	NewCard WLAN

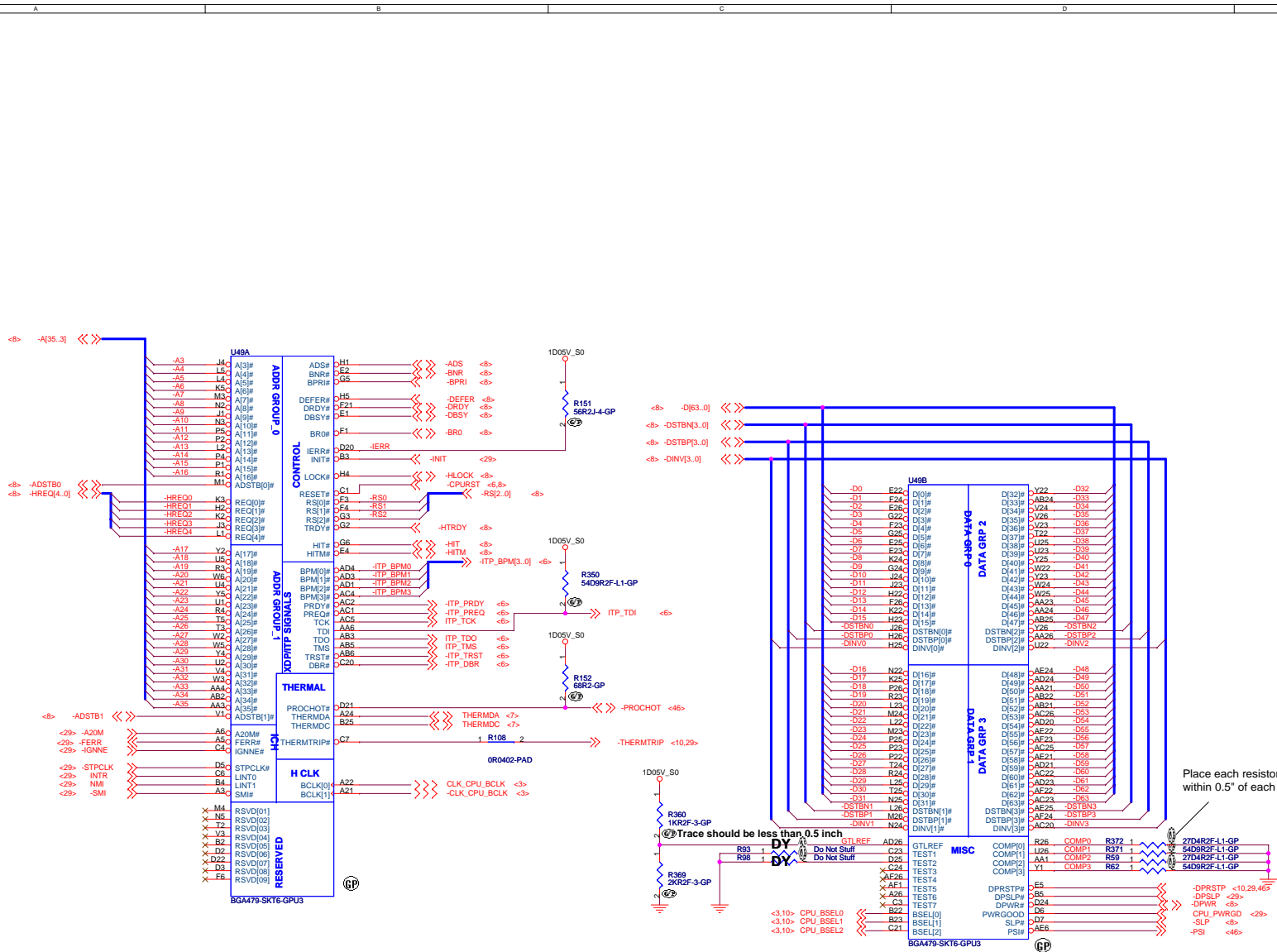


<18,45,46,48,49,50,51,52,53>	DCBATOUT	DCBATOUT
<7,29,39,45,53,55>	3D3V_AUX_S5	3D3V_AUX_S5
<41,45,53>	5V_AUX_S5	5V_AUX_S5
<13,26,27,28,30,31,32,36,38,39,40,42,43,45,50,51,52,53,55>	3D3V_S5	3D3V_S5
<18,30,43,44,45,48,49,50,51,52>	5V_S5	5V_S5
<30,44,52>	1D6V_S3	1D6V_S3
<17,50>	0D9V_S3	0D9V_S3
<51,52>	1D8V_S3	1D8V_S3
<3,7,10,11,13,15,16,18,19,24,25,26,27,28,29,30,31,32,33,34,35,36,39,40,41,42,46,48,52,53,55>	3D3V_S0	3D3V_S0
<7,13,19,22,25,26,30,31,32,35,43,46,52,53,55>	5V_S0	5V_S0
<4,5,6,8,10,11,12,13,29,30,46,48>	1D06V_S0	1D06V_S0
<3,5,13,27,29,30,35,40,41,42,52,55>	1D6V_S0	1D6V_S0
<20,22,23,24,25,52>	1D8V_S0	1D8V_S0
<21,22,24,51>	1D1V_S0	1D1V_S0
<22,24,25,48>	VGA_CORE_S0	VGA_CORE_S0

BOM1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 301, Taiwan, R.O.C.

Reference		
Size C	Document Number	Rev
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Place each resistor within 0.5" of each pin



27D4R2F-L1-GP

54D6R2F-L1-GP

54D6R2F-L1-GP

54D6R2F-L1-GP

54D6R2F-L1-GP

54D6R2F-L1-GP

54D6R2F-L1-GP

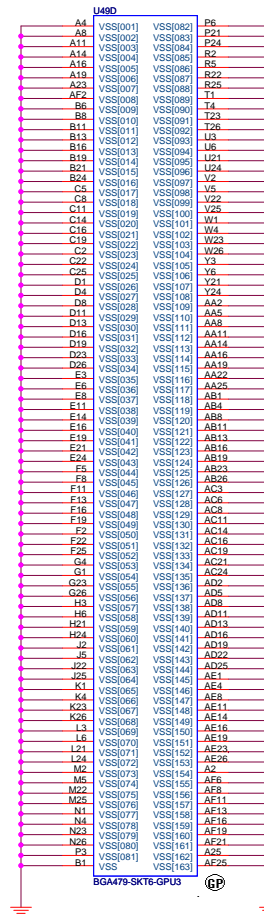
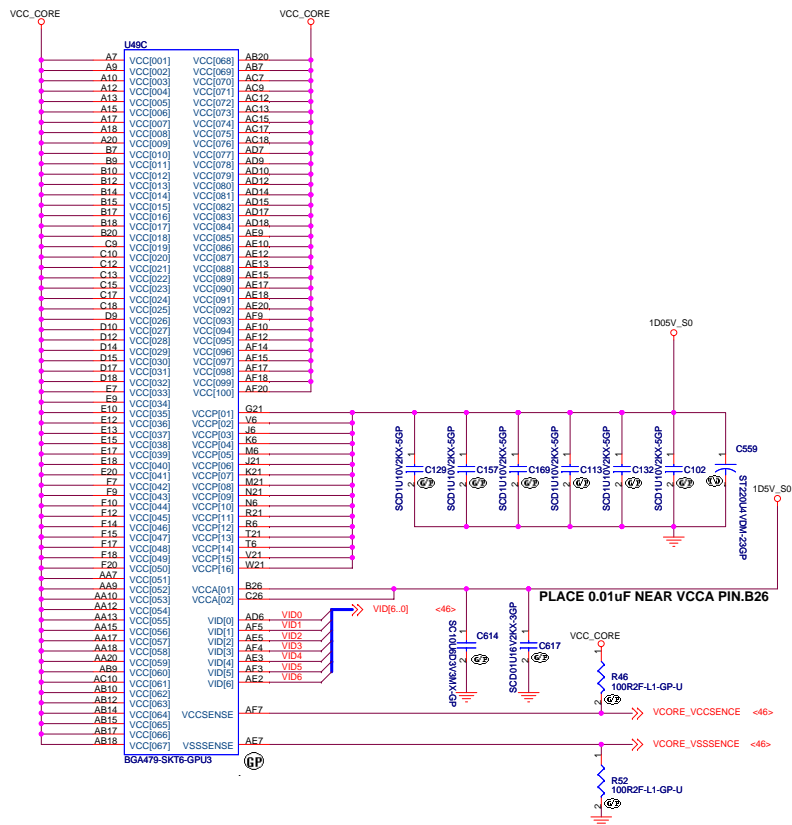
54D6R2F-L1-GP

54D6R2F-L1-GP

54D6R2F-L1-GP

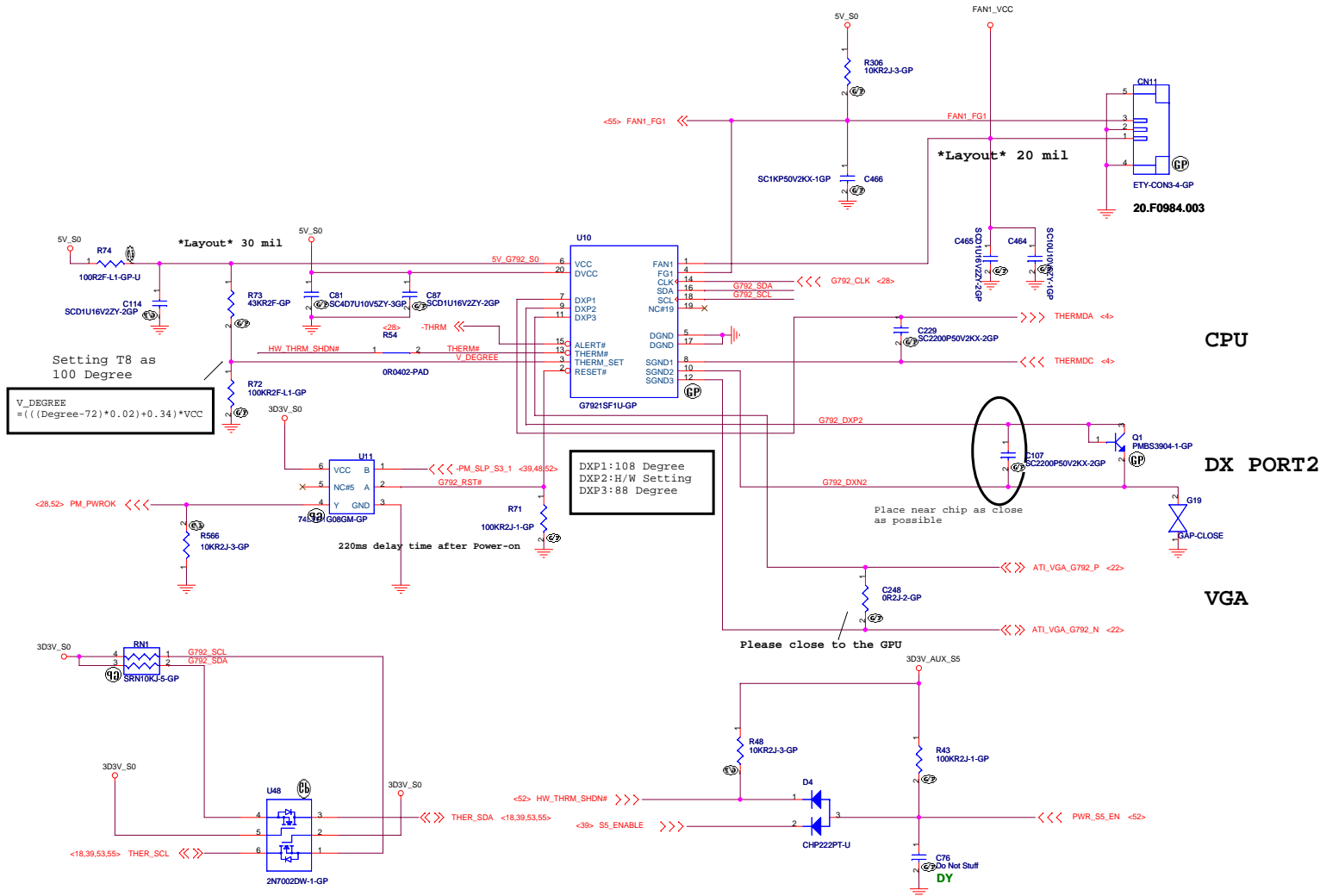
54D6R2F-L1-GP

54D6R2F-L1-GP





- | Ref Des | For ITP.XDP |
|---------|-------------------|
| J1 | NO_ASM->ASM |
| C157 | NO_ASM->ASM |
| R140 | NO_ASM->1K 5% ASM |
| R144 | ASM (No Change) |
| R136 | ASM->NO_ASM |
| R145 | ASM (No Change) |
| R141 | ASM->54.9 1% ASM |
| R143 | ASM->54.9 1% ASM |



CPU

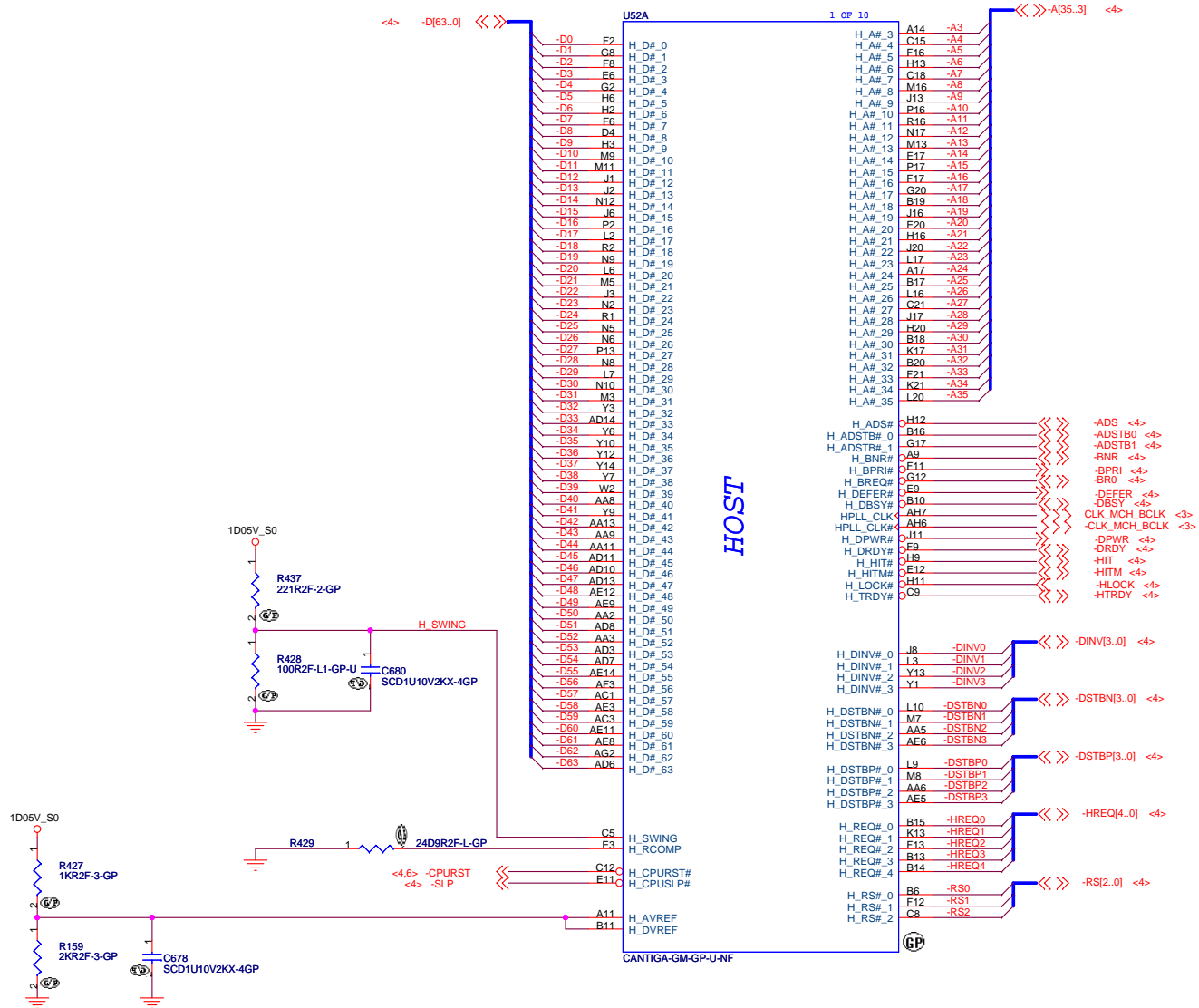
DX PORT2

VGA

BOM1

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Title			
Thermal/Fan Controller G792			
Size	Document Number	Rev	
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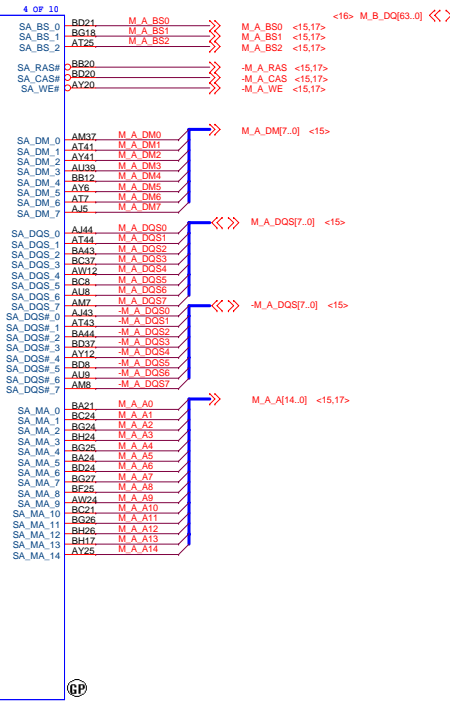
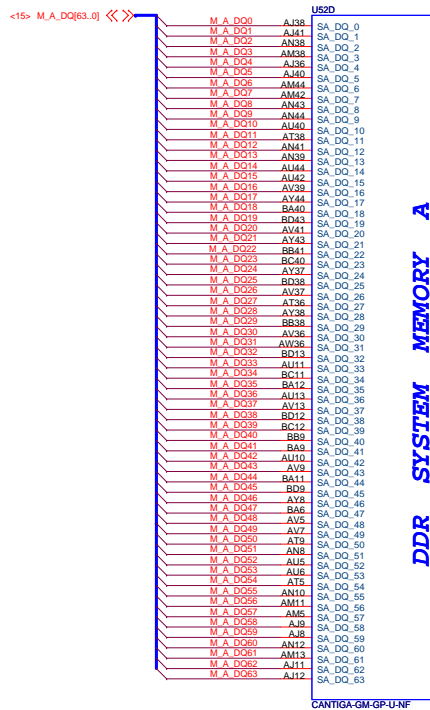
Route H_XSWING & H_YSWING
10 mil wide / 20 mil spacing

Route H_XRCOMP &
H_YRCOMP 10 mil wide /
20 mil spacing

BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title Cantiga(1/7):HOST I/F		
Size A3	Document Number LT32M	Rev -3
Date: Monday, July 07, 2008	Sheet 8 of 54	

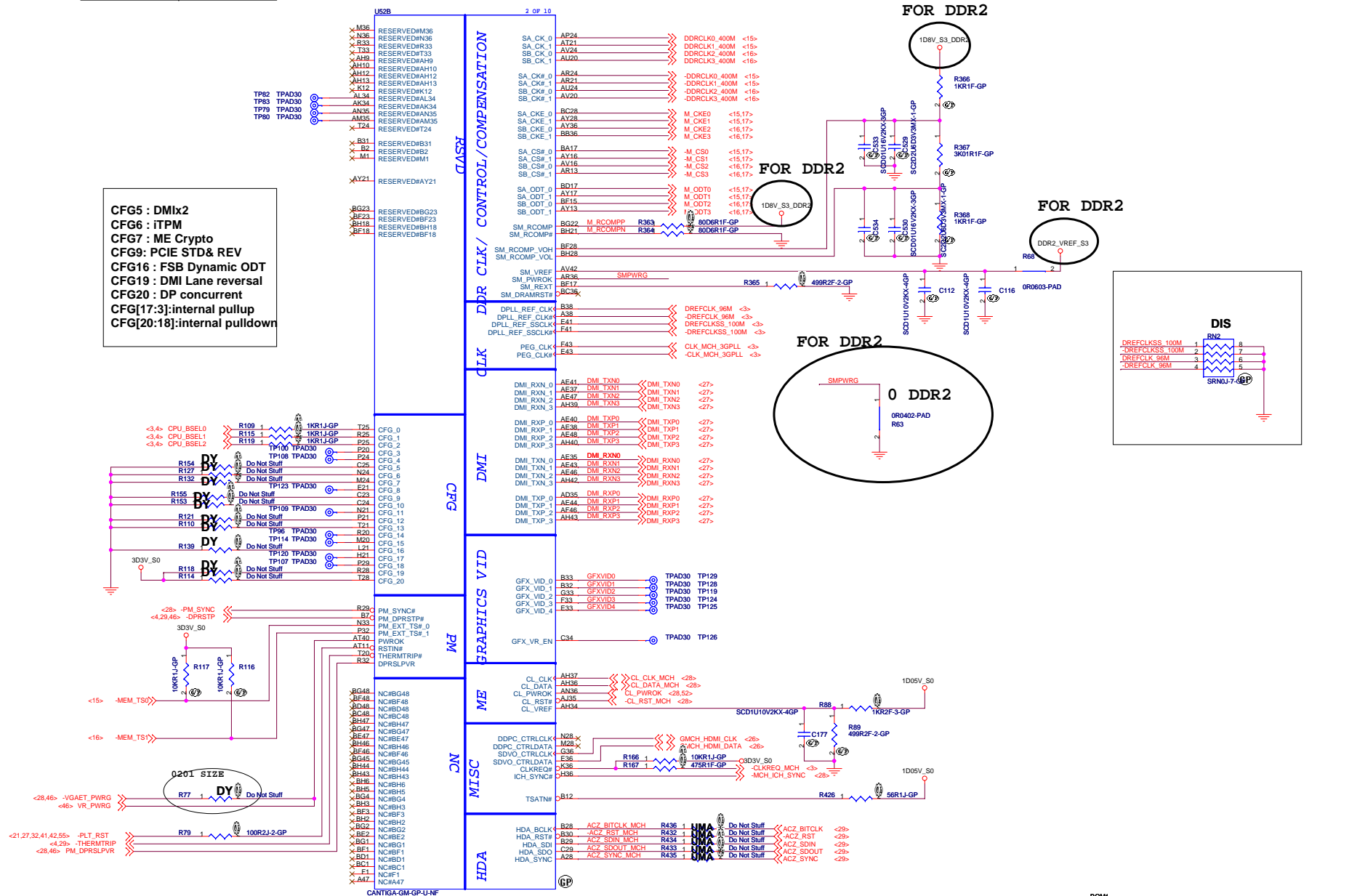


BOH1

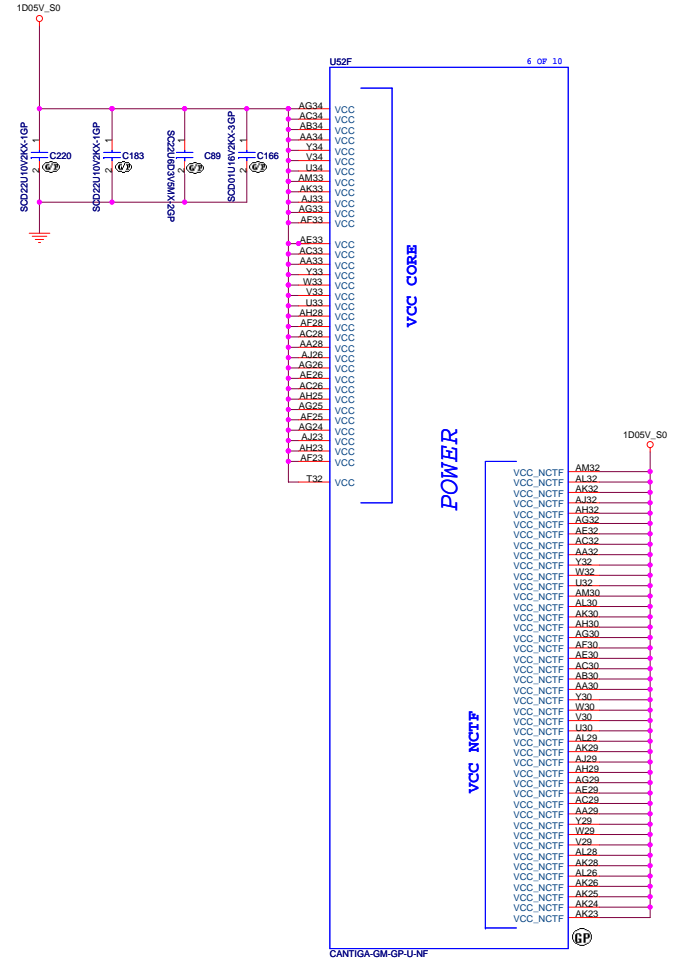
緯創資通 Wistron Corporation
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Taippei Hsien 221, Taiwan, R.O.C.

File Cantiga(2/7):DDR3
Size C Document Number LT32M Rev -3
Date: Monday, July 07, 2008 Sheet 9 of 54

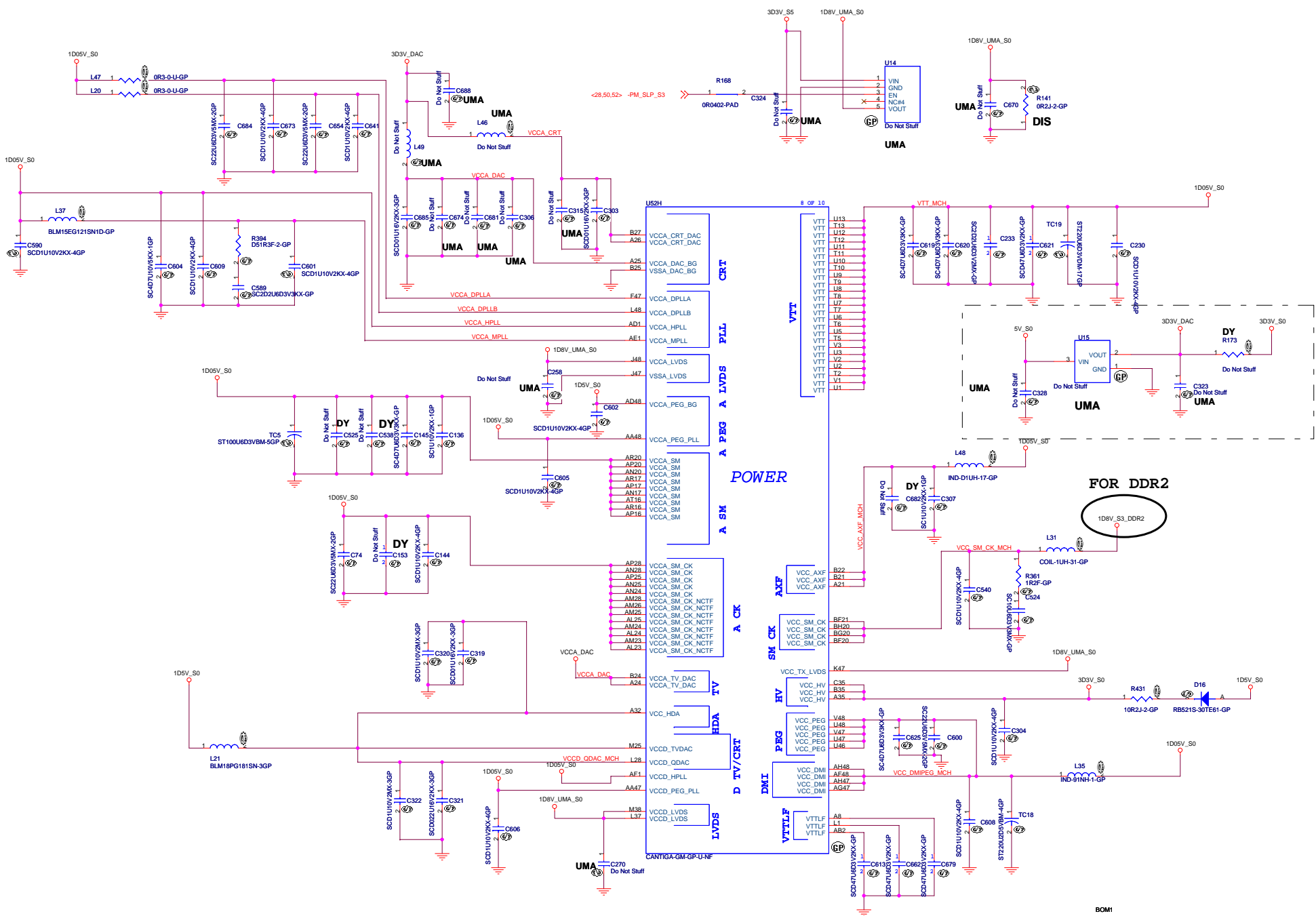
RESERVED#AL34	ME_JTAG_TCK
RESERVED#AK34	ME_JTAG_TDI
RESERVED#AN35	ME_JTAG_TDO
RESERVED#AM35	ME_JTAG_TMS



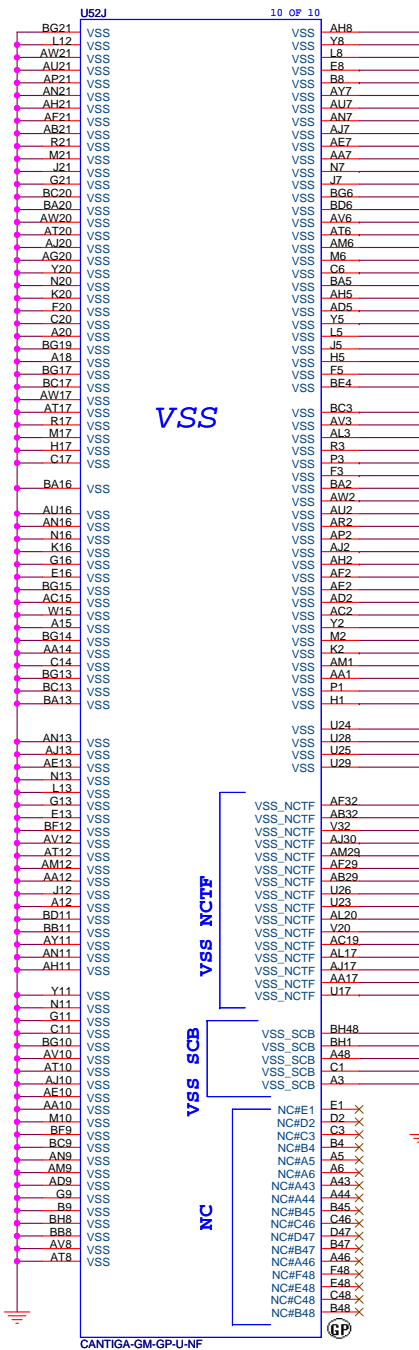
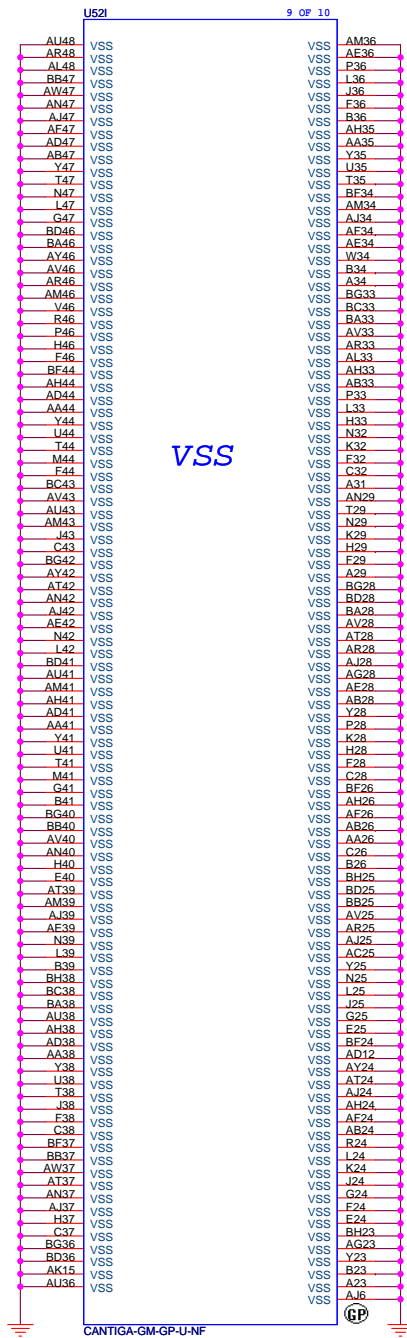
1D8V_S3_DDR2



BOM1			
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Title			
Cantiga(5/7):VCC			
Size C	Document Number		Rev -3
LT32M			
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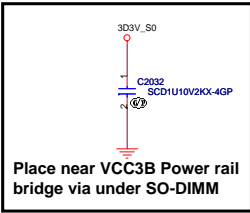


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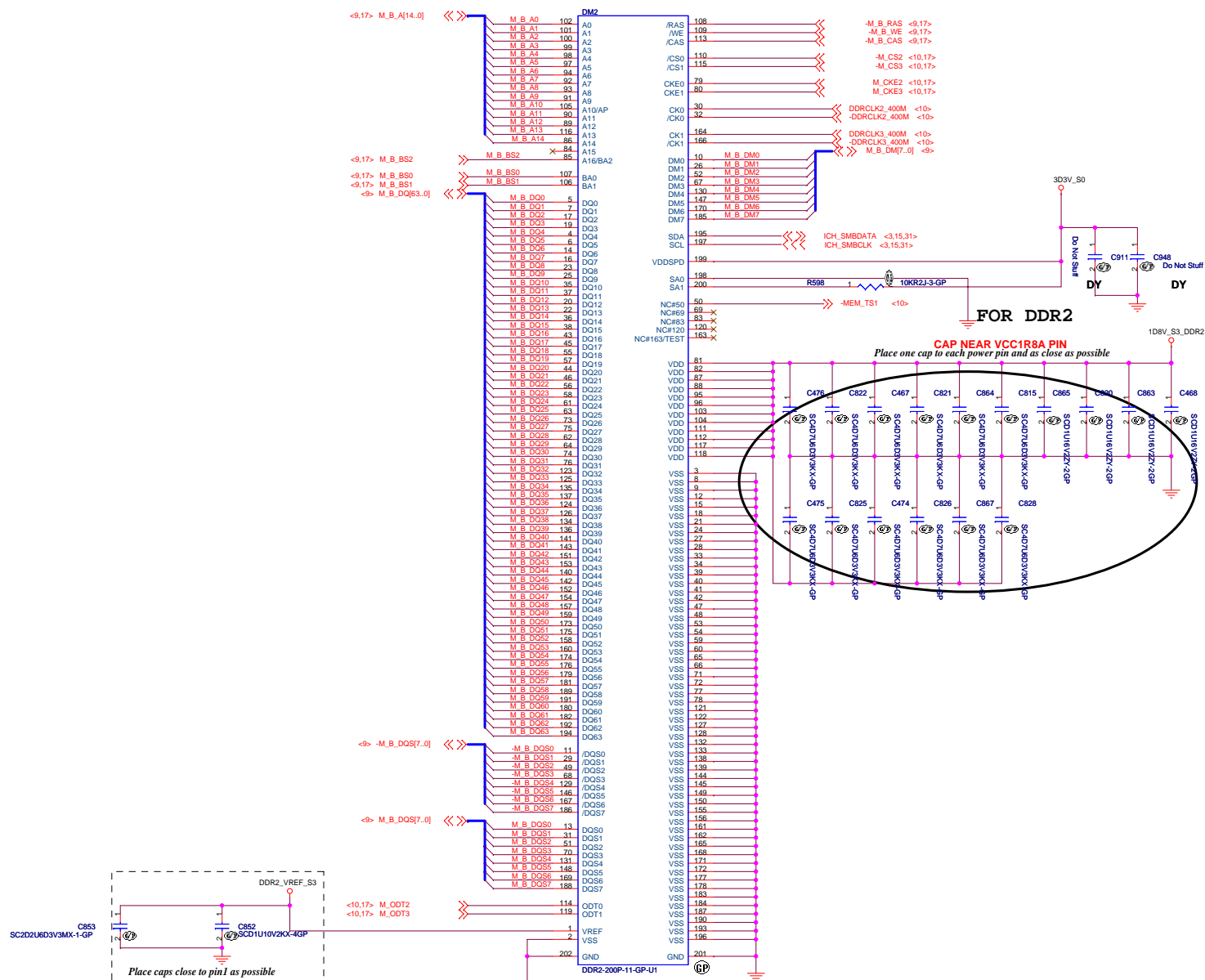
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緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Cantiga(8/7):GND	
Size A3	Document Number LT32M
Date: Monday, July 07, 2008	Sheet 14 of 54
Rev -3	



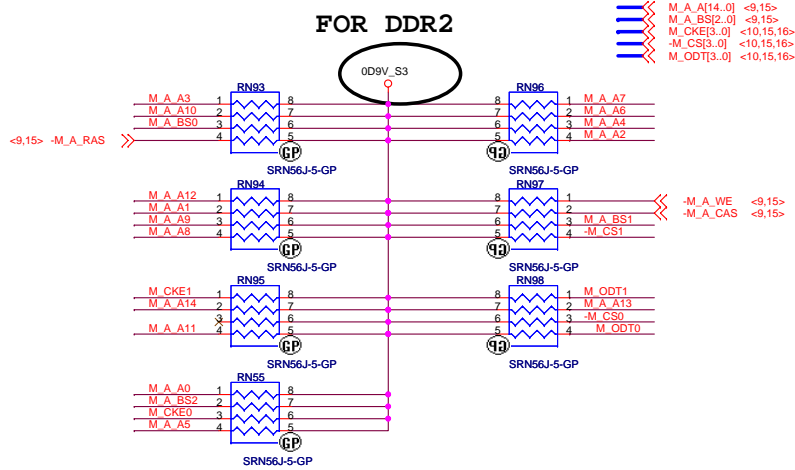
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Title			
DDR2 SODIMM-A			
Size	Document Number		Rev
C		LT32M	-3
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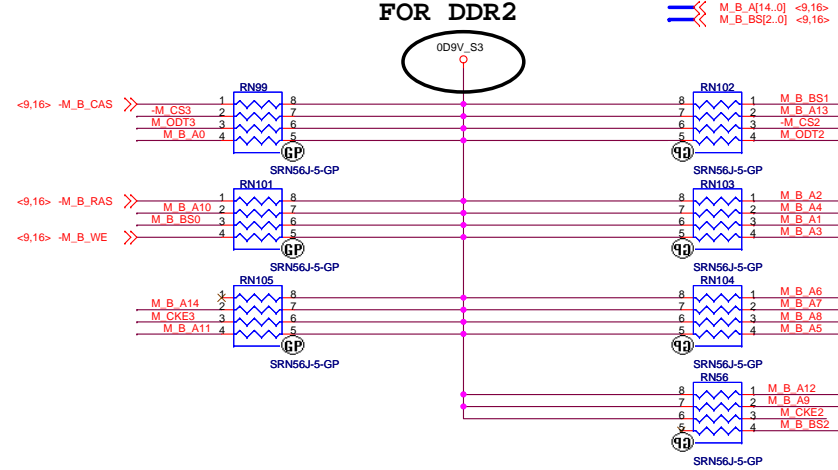
CHANNEL A PARALLEL TERMINATION

FOR DDR2



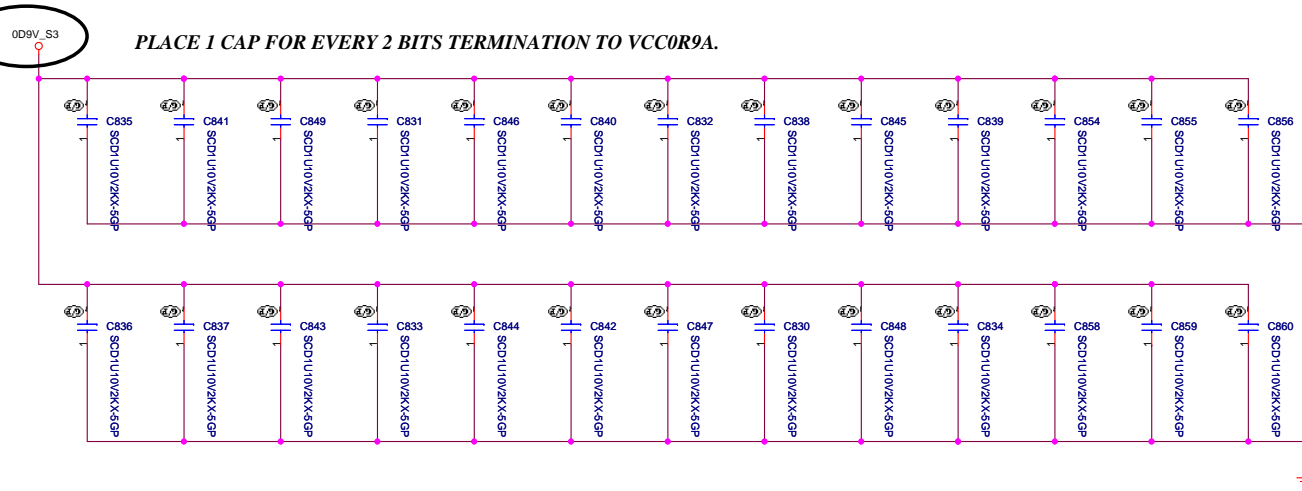
CHANNEL B PARALLEL TERMINATION

FOR DDR2



FOR DDR2

PLACE 1 CAP FOR EVERY 2 BITS TERMINATION TO VCC0R9A.

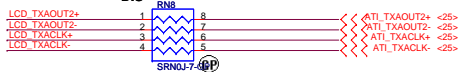
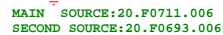


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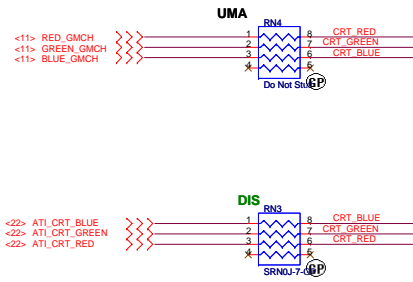
緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title	DDR-2 TERMINATION/DECOUPLING		
Size	Document Number	Rev	-3
Custom	LT32M		
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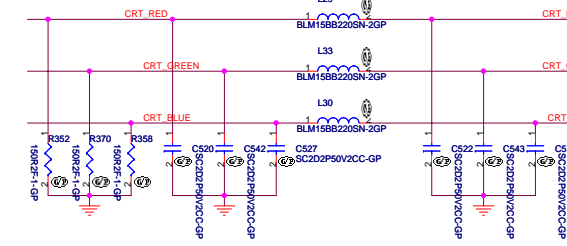
[illegible]

CRT I/F & CONNECTOR

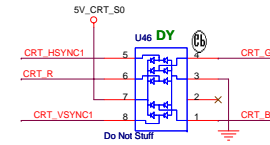
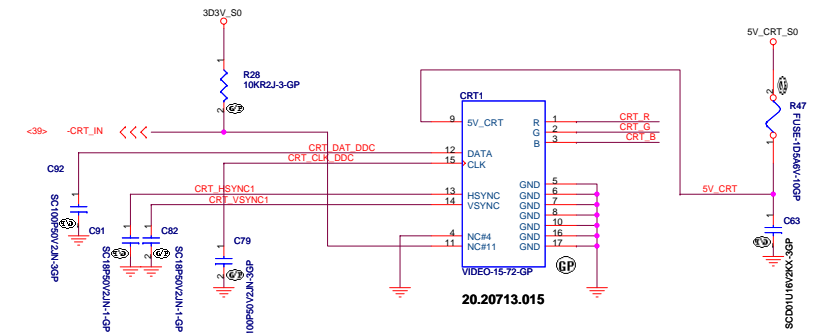


Layout Note:
Place these resistors
close to the CRT-out
connector

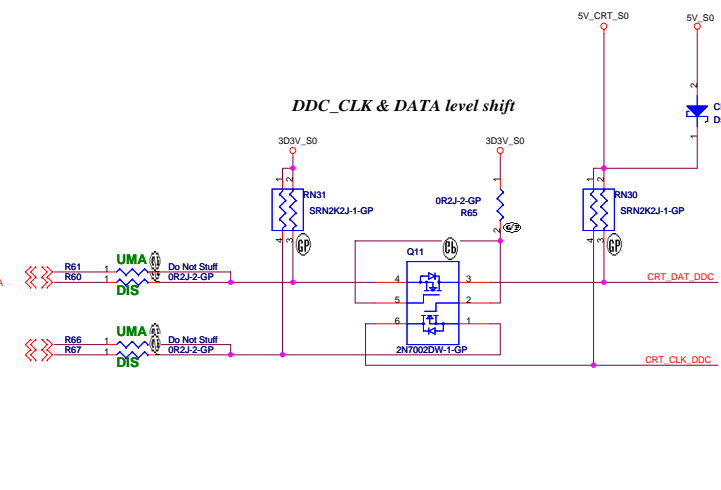
Ferrite bead impedance: 10 ohm@100MHz



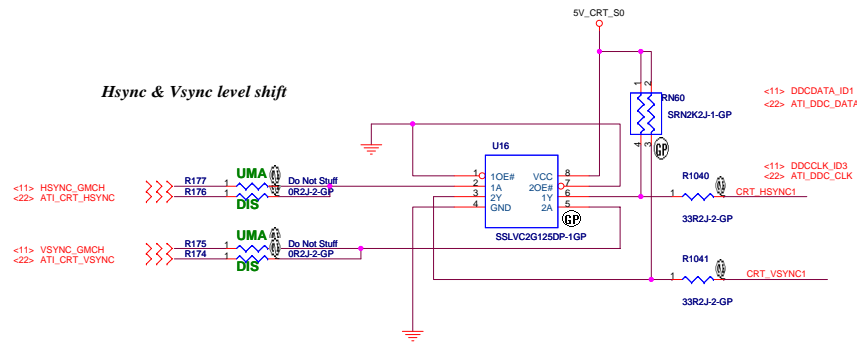
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



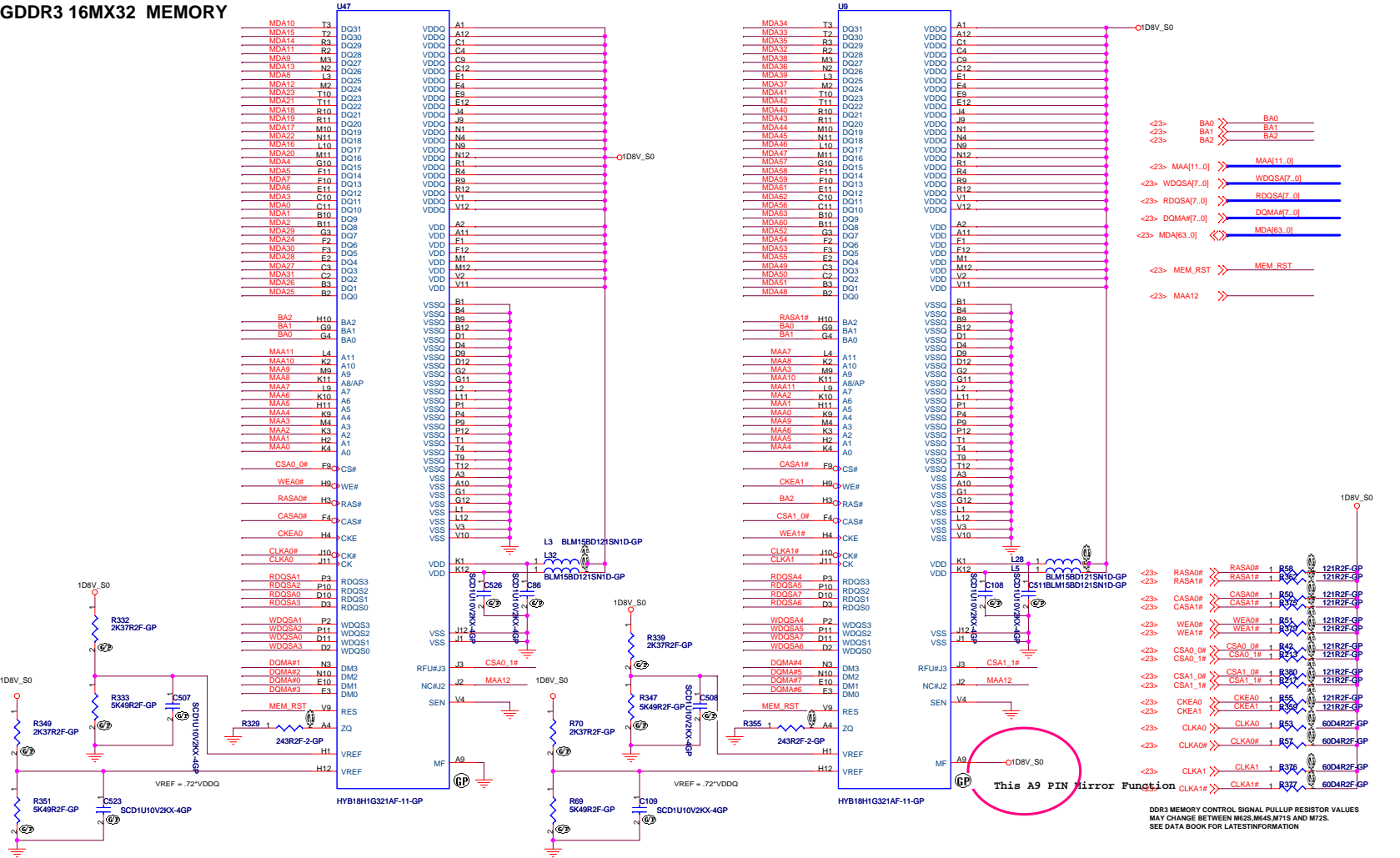
DDC_CLK & DATA level shift



Hsync & Vsync level shift



GDDR3 16MX32 MEMORY



PLACE VREF DIVIDER COMPONENTS AS CLOSE TO MEMORY AS POSSIBLE

Pin	Signal	Pin	Signal
C488	SCD1U10V2KX-4GP	C515	SCD1U10V2KX-4GP
C502	SCD1U10V2KX-4GP	C516	SCD1U10V2KX-4GP
C544	SCD1U10V2KX-4GP	C517	SCD1U10V2KX-4GP
C506	SCD1U10V2KX-4GP	C518	SCD1U10V2KX-4GP
C101	SCD1U10V2KX-4GP	C519	SCD1U10V2KX-4GP
C123	SCD1U10V2KX-4GP	C520	SCD1U10V2KX-4GP
C06	SCD1U10V2KX-4GP	C521	SCD1U10V2KX-4GP
C08	SCD1U10V2KX-4GP	C522	SCD1U10V2KX-4GP
C94	SCD1U10V2KX-4GP	C523	SCD1U10V2KX-4GP
C09	SCD1U10V2KX-4GP	C524	SCD1U10V2KX-4GP
C538	SCD1U10V2KX-4GP	C525	SCD1U10V2KX-4GP
C510	SCD1U10V2KX-4GP	C526	SCD1U10V2KX-4GP
C511	SCD1U10V2KX-4GP	C527	SCD1U10V2KX-4GP
C512	SCD1U10V2KX-4GP	C528	SCD1U10V2KX-4GP
C513	SCD1U10V2KX-4GP	C529	SCD1U10V2KX-4GP
C514	SCD1U10V2KX-4GP	C530	SCD1U10V2KX-4GP
C515	SCD1U10V2KX-4GP	C531	SCD1U10V2KX-4GP
C516	SCD1U10V2KX-4GP	C532	SCD1U10V2KX-4GP
C517	SCD1U10V2KX-4GP	C533	SCD1U10V2KX-4GP
C518	SCD1U10V2KX-4GP	C534	SCD1U10V2KX-4GP
C519	SCD1U10V2KX-4GP	C535	SCD1U10V2KX-4GP
C520	SCD1U10V2KX-4GP	C536	SCD1U10V2KX-4GP
C521	SCD1U10V2KX-4GP	C537	SCD1U10V2KX-4GP
C522	SCD1U10V2KX-4GP	C538	SCD1U10V2KX-4GP
C523	SCD1U10V2KX-4GP	C539	SCD1U10V2KX-4GP
C524	SCD1U10V2KX-4GP	C540	SCD1U10V2KX-4GP
C525	SCD1U10V2KX-4GP	C541	SCD1U10V2KX-4GP
C526	SCD1U10V2KX-4GP	C542	SCD1U10V2KX-4GP
C527	SCD1U10V2KX-4GP	C543	SCD1U10V2KX-4GP
C528	SCD1U10V2KX-4GP	C544	SCD1U10V2KX-4GP
C529	SCD1U10V2KX-4GP	C545	SCD1U10V2KX-4GP
C530	SCD1U10V2KX-4GP	C546	SCD1U10V2KX-4GP
C531	SCD1U10V2KX-4GP	C547	SCD1U10V2KX-4GP
C532	SCD1U10V2KX-4GP	C548	SCD1U10V2KX-4GP
C533	SCD1U10V2KX-4GP	C549	SCD1U10V2KX-4GP
C534	SCD1U10V2KX-4GP	C550	SCD1U10V2KX-4GP

BOM1

緯創資通 Wistron Corporation		
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ATI M82-S VRAM(1,2)		
Size	Document Number	Rev
C	LT32M	-3
Date: Monday, July 07, 2008	Sheet 20 of 54	

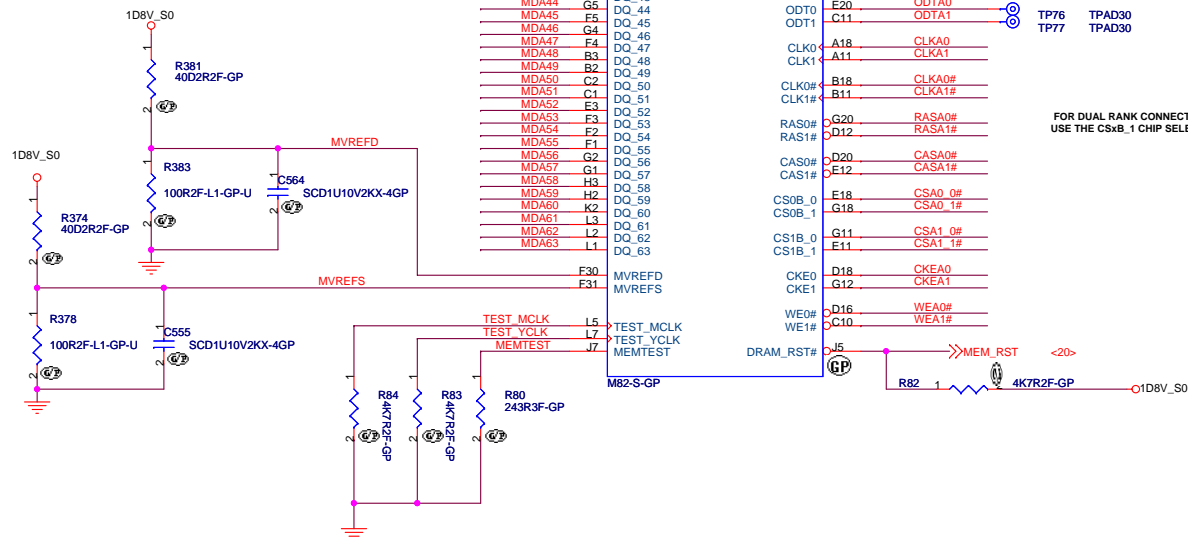
<20> RASA0# <<> RASA0#
 <20> RASA1# <<> RASA1#
 <20> CASA0# <<> CASA0#
 <20> CASA1# <<> CASA1#
 <20> WEA0# <<> WEA0#
 <20> WEA1# <<> WEA1#
 <20> CKEA0 <<> CKEA0
 <20> CKEA1 <<> CKEA1
 <20> CSA0_0# <<> CSA0_0#
 <20> CSA1_0# <<> CSA1_0#
 <20> CSA0_1# <<> CSA0_1#
 <20> CSA1_1# <<> CSA1_1#

<20> CLKA0 <<> CLKA0
 <20> CLKA0# <<> CLKA0#
 <20> CLKA1 <<> CLKA1
 <20> CLKA1# <<> CLKA1#
 <20> <<> WDQSA[7..0]
 <20> <<> RDQSA[7..0]
 <20> <<> DQMA#[7..0]
 <20> <<> MDA[63..0]
 <20> <<> MAA[11..0]

<20> BA0 <<> BA0
 <20> BA1 <<> BA1
 <20> BA2 <<> BA2
 <20> MAA12 <<> MAA12

PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC

DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

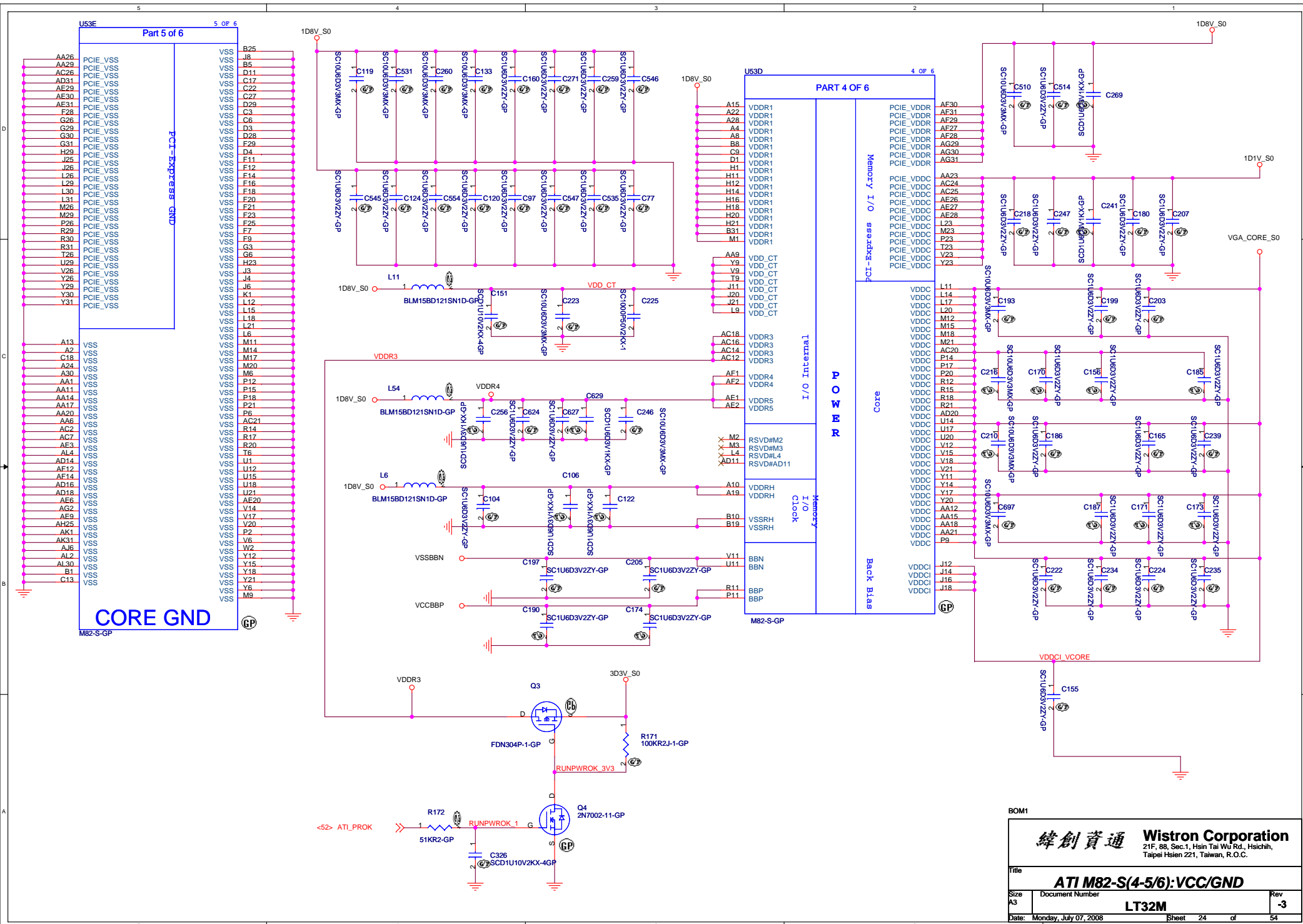


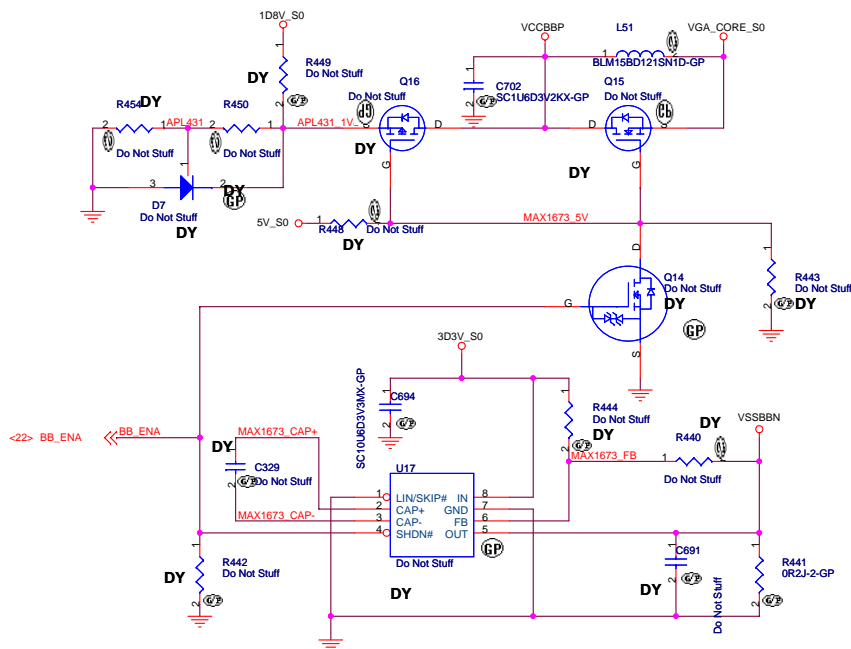
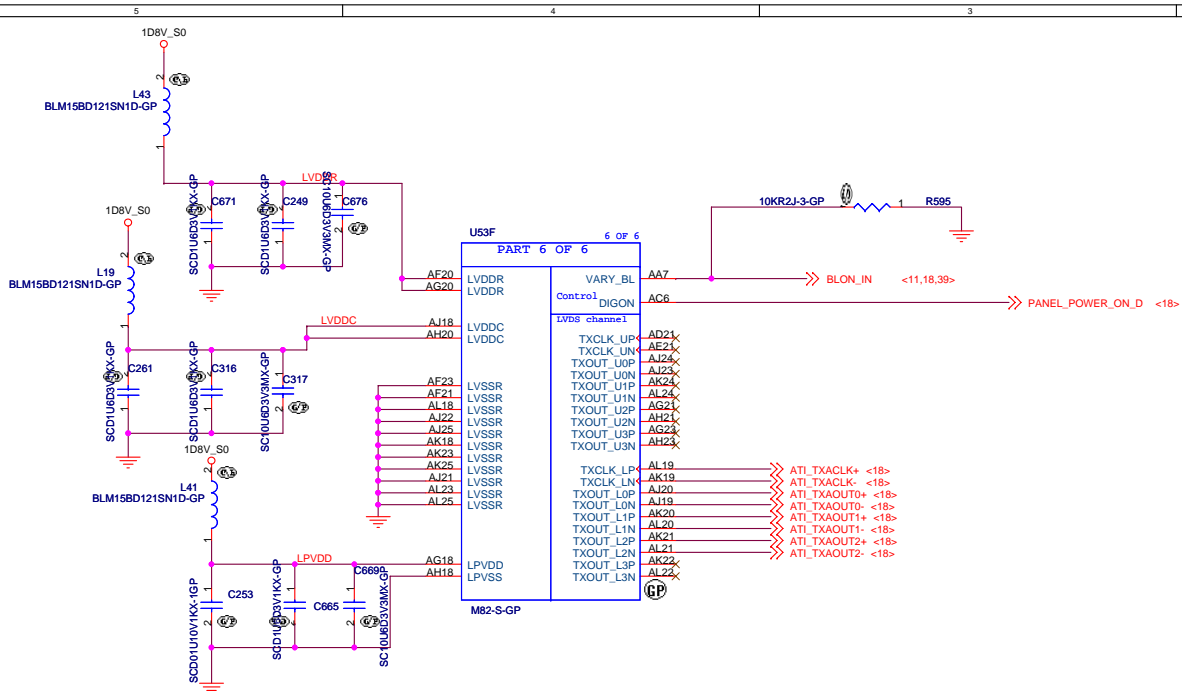
BOM1

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

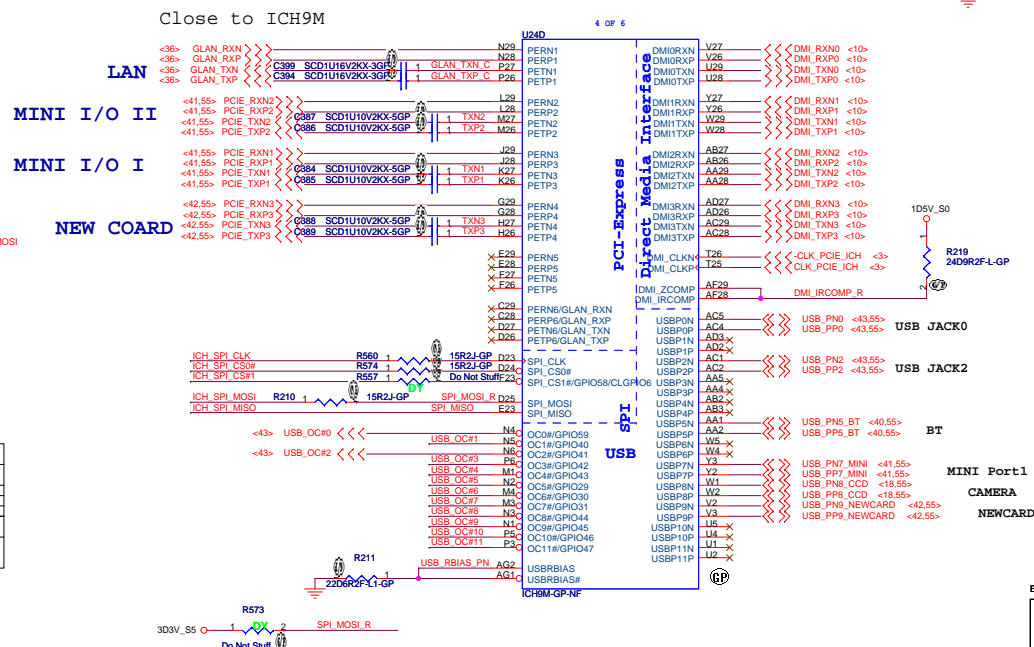
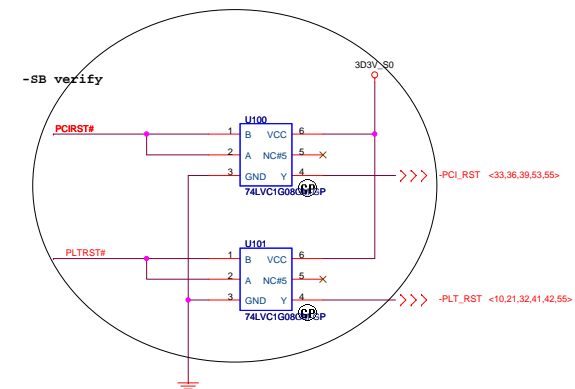
Title **ATI M82-S(3/6):Memory Interface**

Size A3 Document Number **LT32M** Rev **-3**
 Date: Monday, July 07, 2008 Sheet 23 of 54





緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
ATI M82-S(6/6):LVDS		
Title Size Custom	Document Number LT32M	Rev -3
Date: Monday, July 07, 2008	Sheet 25 of 54	

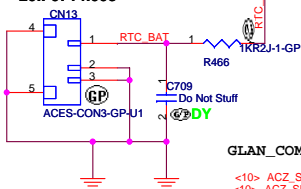


The diagram shows three signal traces: PCI_GNT#0, ICH_SPI_CS#1, and PCI_GNT#3. Each trace has a green 'DY' label and a blue 'Do Not Stuff' label. The traces are connected to a common ground symbol.

Title			
ICH9-M (1 of 4)			
Size	Document Number		Rev
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MAIN SOURCE:20.F0411.003
SECOND SOURCE:20.D0246.103

20.F0714.003



GLAN_COMP place within 500 mils of ICH9M

<10> ACZ_SDIN
<10> ACZ_SDOOUT
<10> ACZ_SYNC
<10> ACZ_RST
<10> ACZ_BITCLK

Do Not Stuff
Do Not Stuff

<40,55> ACZ_BITCLK_MDC
<35> ACZ_BITCLK_RTL
<35> ACZ_SYNC_RTL
<40,55> ACZ_SYNC_MDC
<40,55> ACZ_RST_MDC
<35> ACZ_RST_RTL

<35> ACZ_SDATIN_RTL
<40,55> ACZ_SDATIN_MDC
<40,55> ACZ_SDATIN_OUT_MDC
<35> ACZ_SDATIN_OUT_RTL

<53> SATA_LED#

<32,55> SATA_RXN0

<32,55> SATA_RXP0

<32,55> SATA_TXN0

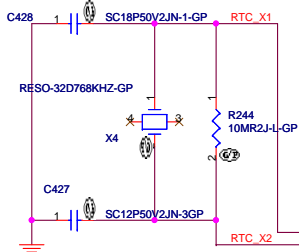
<32,55> SATA_TXP0

<32,55> SATA_RXN1

<32,55> SATA_RXP1

<32,55> SATA_TXN1

<32,55> SATA_TXP1



KDS: RESO 32.768KHZ / 12P

U24A 1 OF 6

RTC_X1
RTC_X2

RTC_RST#
SRTC_RST#
INTRUDER#

INTVRMEN
LAN100_SLP

GLAN_CLK
LAN_RSTSYNC

LAN_RXD0
LAN_RXD1
LAN_RXD2

LAN_TXD0
LAN_TXD1
LAN_TXD2

GLAN_COMP
GLAN_COMPO

GLAN_COMPO
GLAN_COMPO

HDA_RST#
HDA_RST#

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HDA_RST#

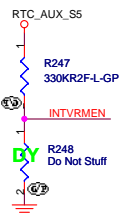
HDA_RST#
HDA_RST#

HDA_RST#
HDA_RST#

HDA_RST#
HDA_RST#

HDA_RST#
HDA_RST#

Integrated VccSus1_05,VccSus1_5,VccCl1_5	
INTVRMEN	High=Enable Low=Disable
Integrated VccLan1_05VccCl1_05	
LAN100_SLP	High=Enable Low=Disable



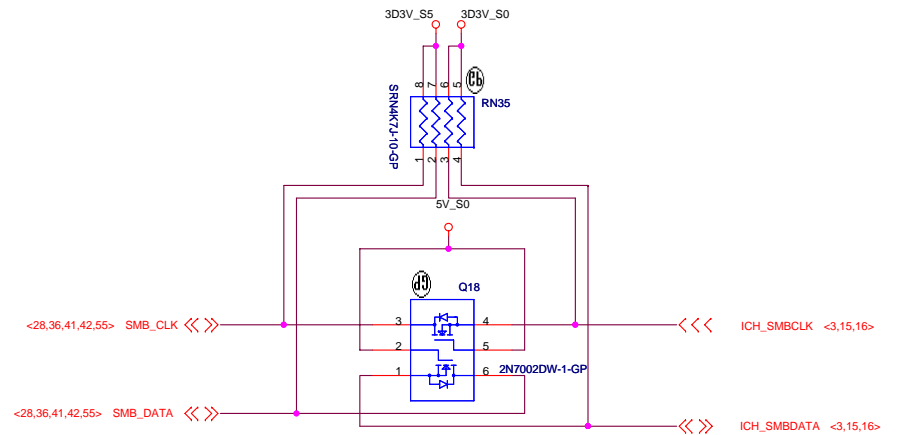
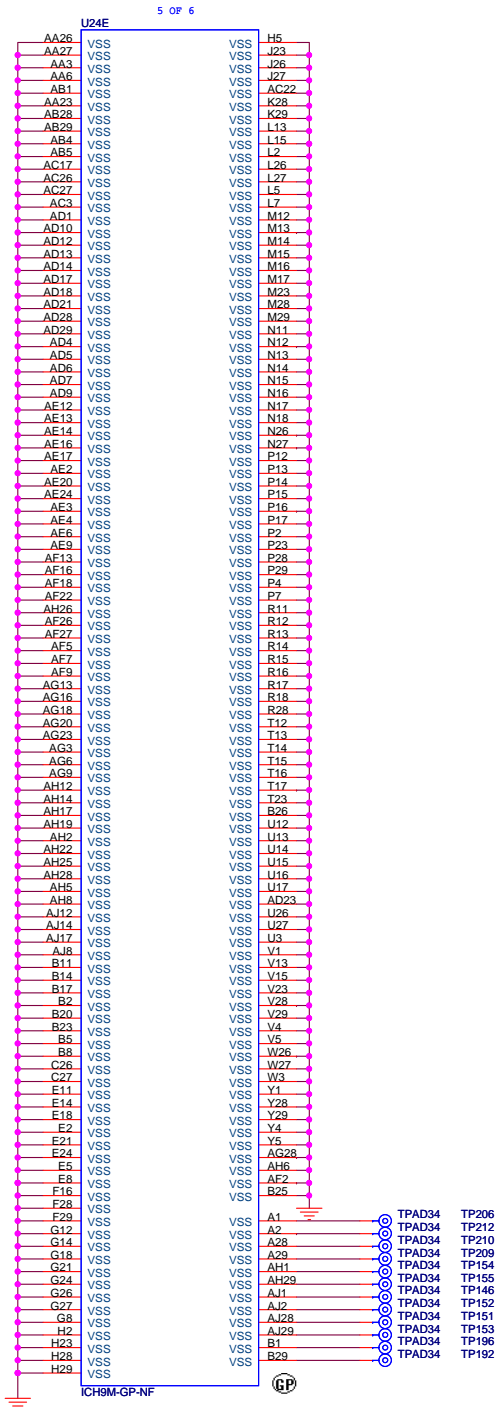
Place within 500 mils of ICH9 ball

Layout note: R373 needs to be placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub

BOM1

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Size	Document Number	Rev
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Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

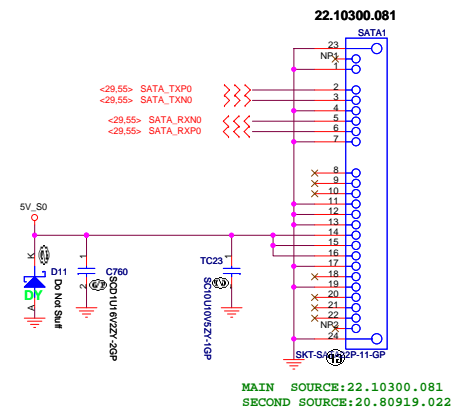
SMBUS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

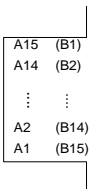
Title		ICH9-M (4 of 4)	
Size	Document Number	Rev	
LT32M		-3	
Date: Monday, July 07, 2008	Sheet 31 of 54		

SATA HD Connector

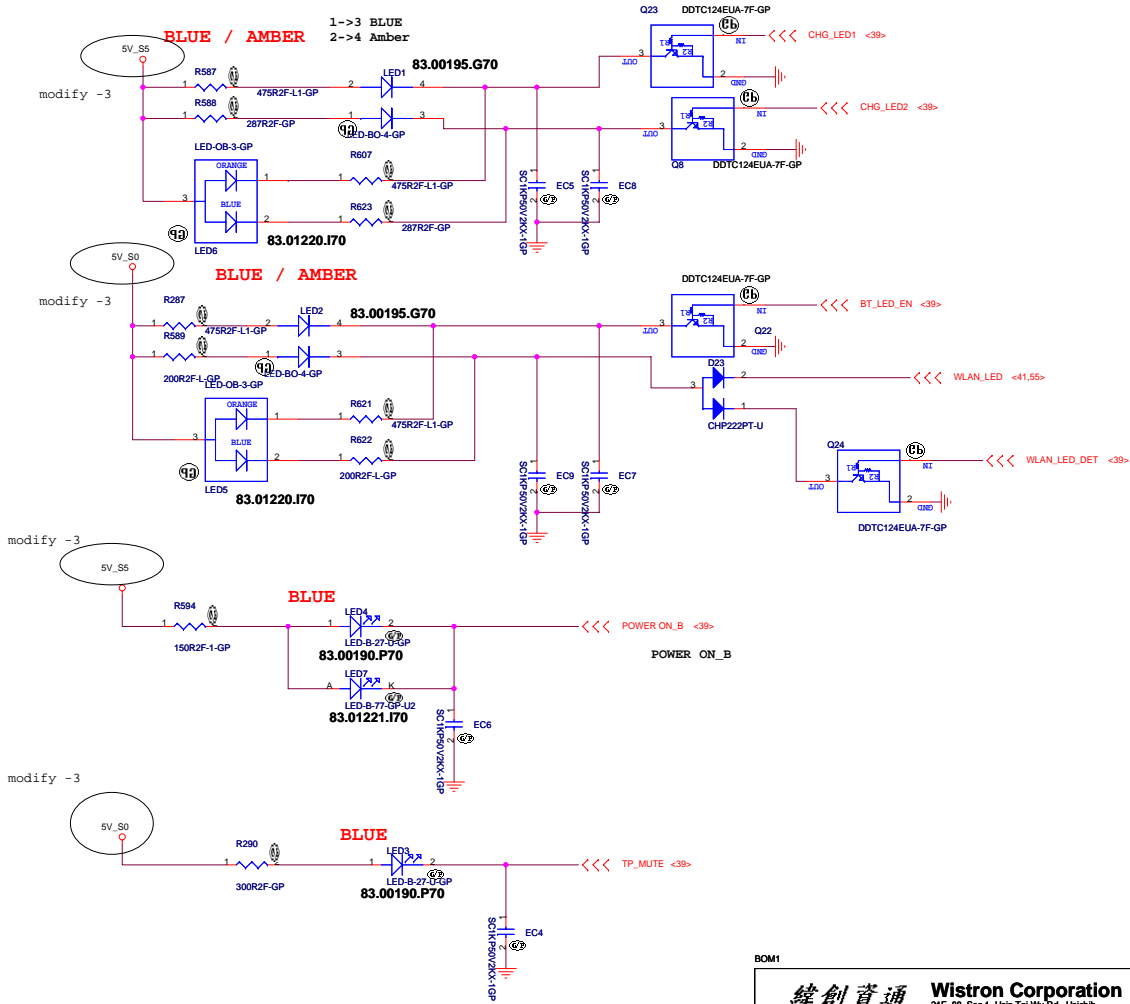
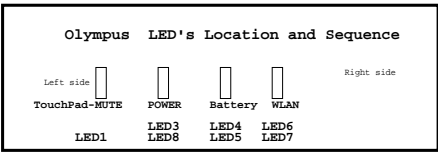
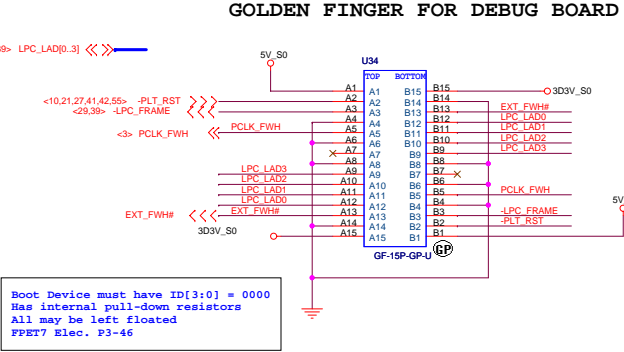
ODD Connector

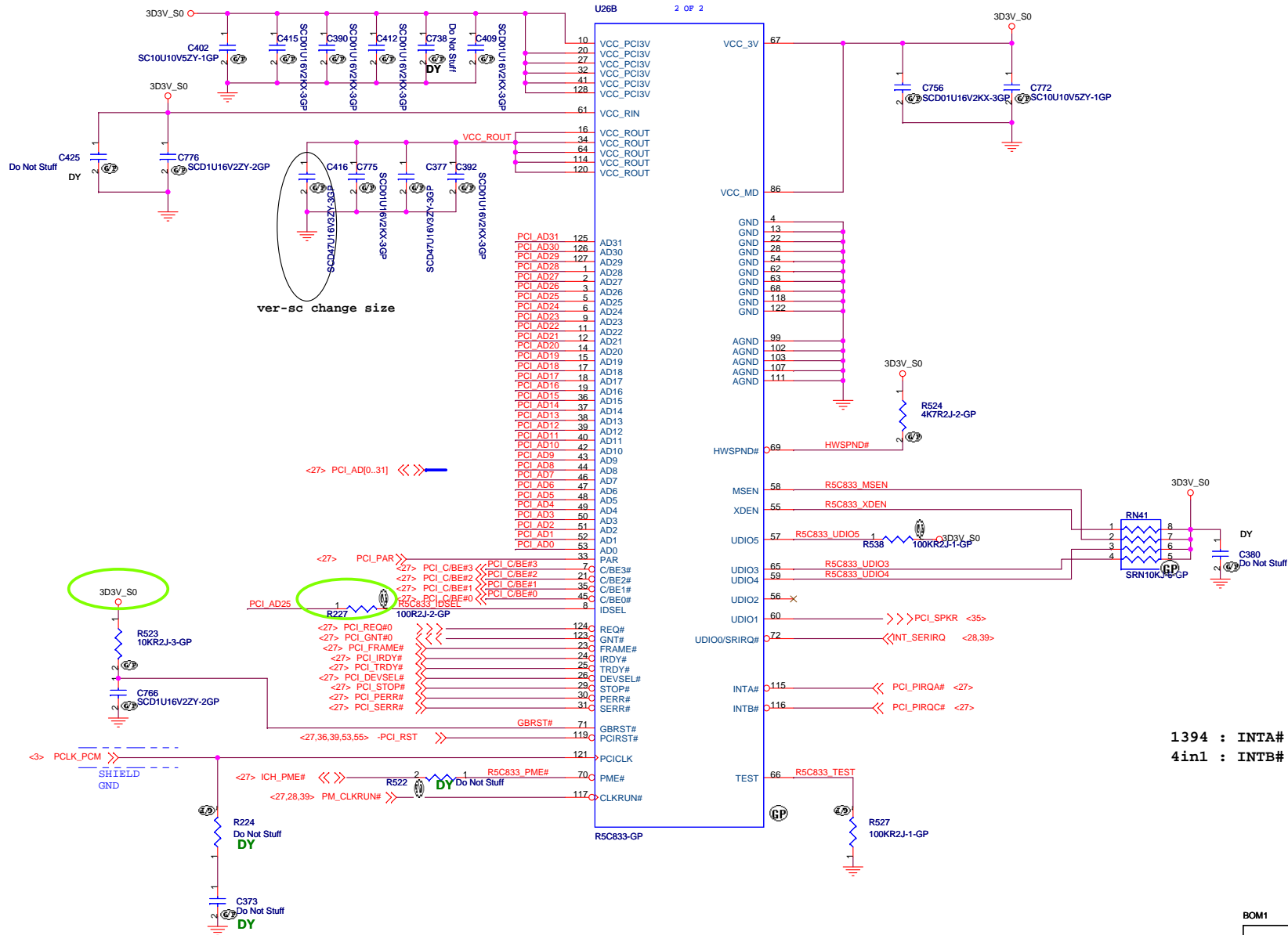


TOP VIEW



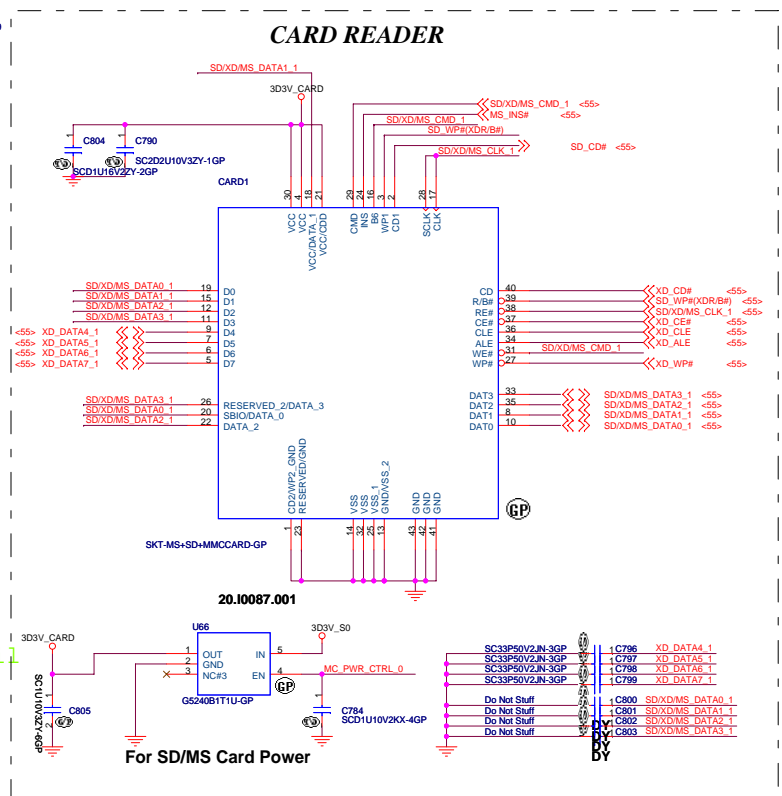
(BOTTOM VIEW)

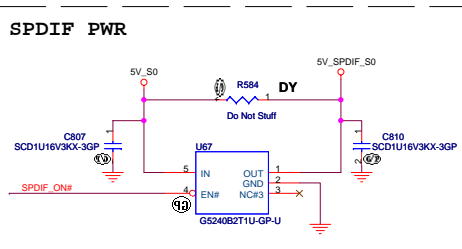
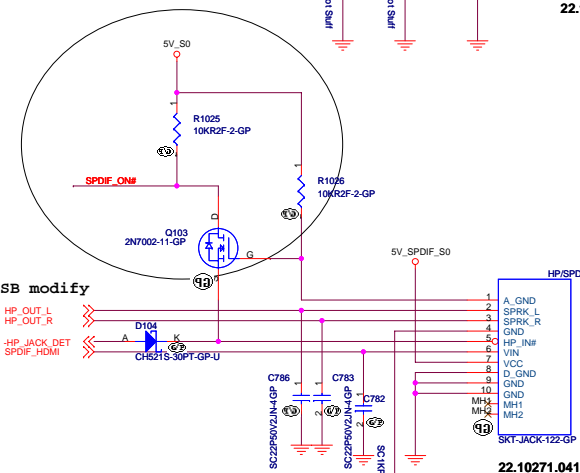
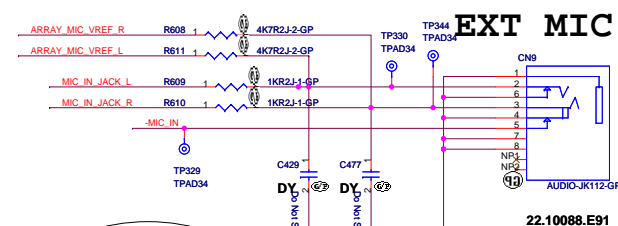
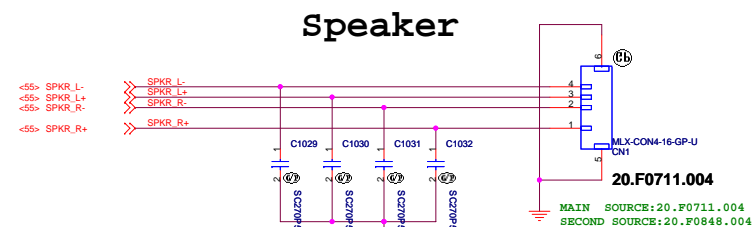




BOM1

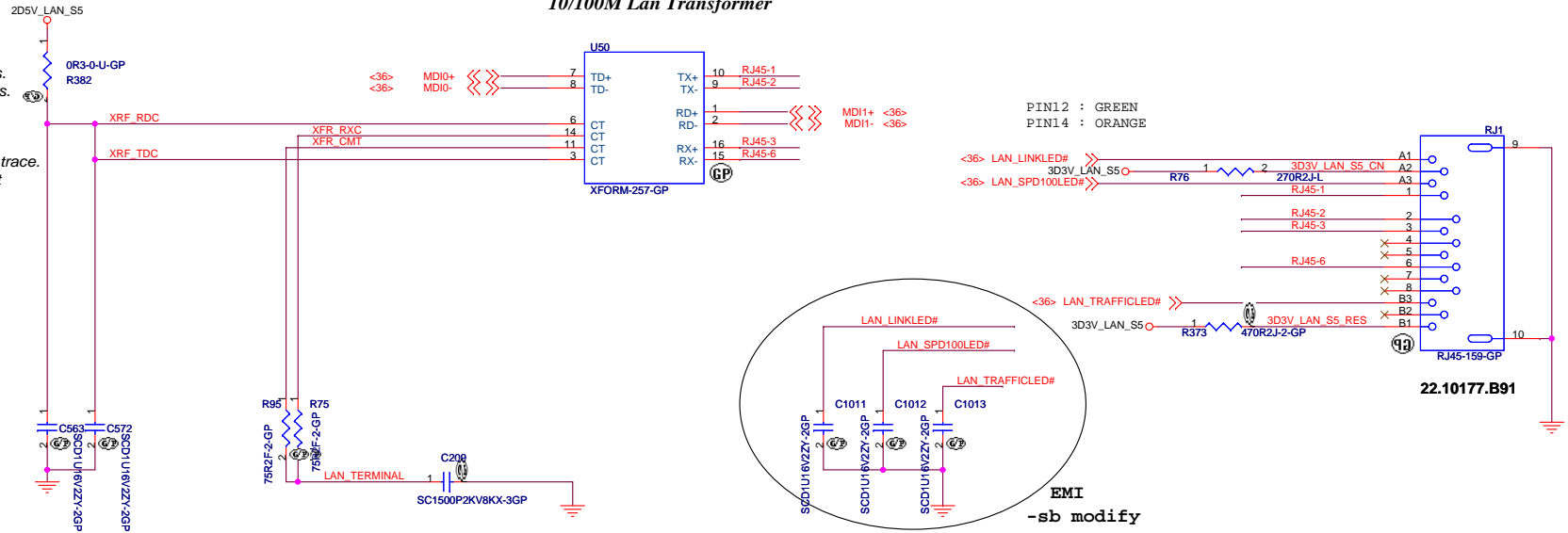
緯創資通		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
R5C832/PCI			
Size	Document Number	Rev	
A3	LT32M	-3	
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10/100M Lan Transformer

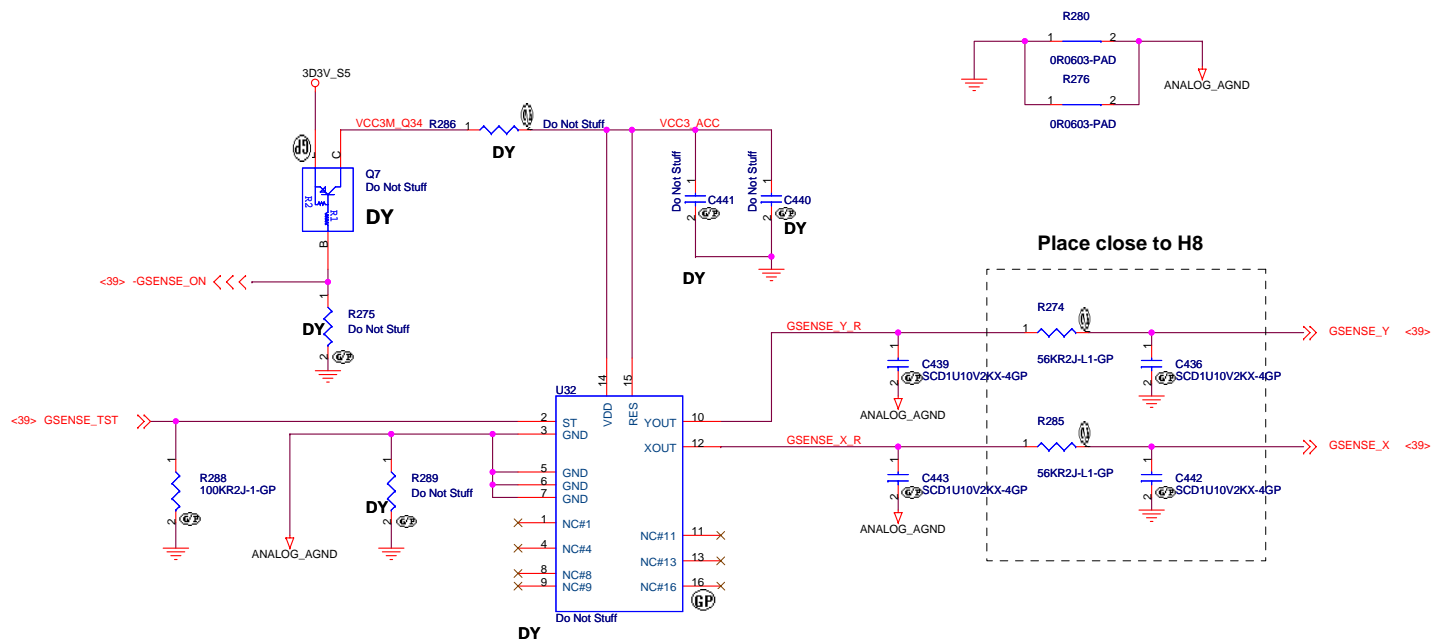
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.



BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title			
LAN connector/NEW CARD/SIM			
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Date: Monday, July 07, 2008		Sheet 37 of 54	



Primary : STMicro LIS244AL
2nd: ADI ADXL322

Width = 6 mil & Spacing = 10 mil
for three Output traces

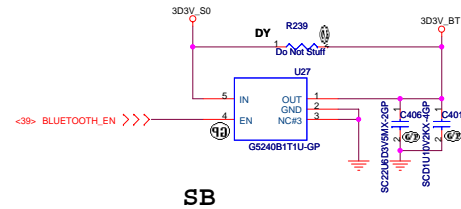
	ADXL322 LIS244AL	No Accel
R545	NO_ASM	ASM
R547	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

- (1) Place C439, C443, Q7, R286, R275, C441, C440, R288, R289 close to U32.
- (2) Avoid routing under DCDC switching area.

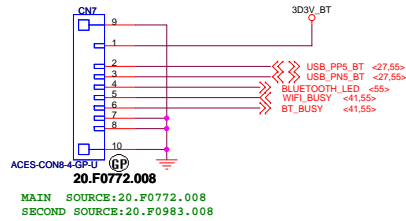
BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title G-SENSOR		
Size A3	Document Number LT32M	Rev -3
Date: Monday, July 07, 2008	Sheet 38 of 54	

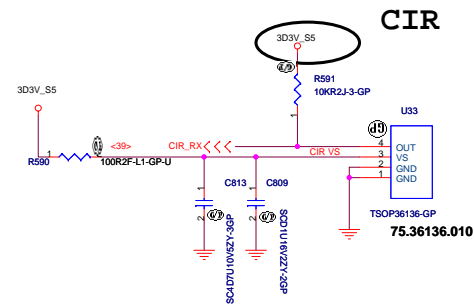


SB

BT CONNECTOR

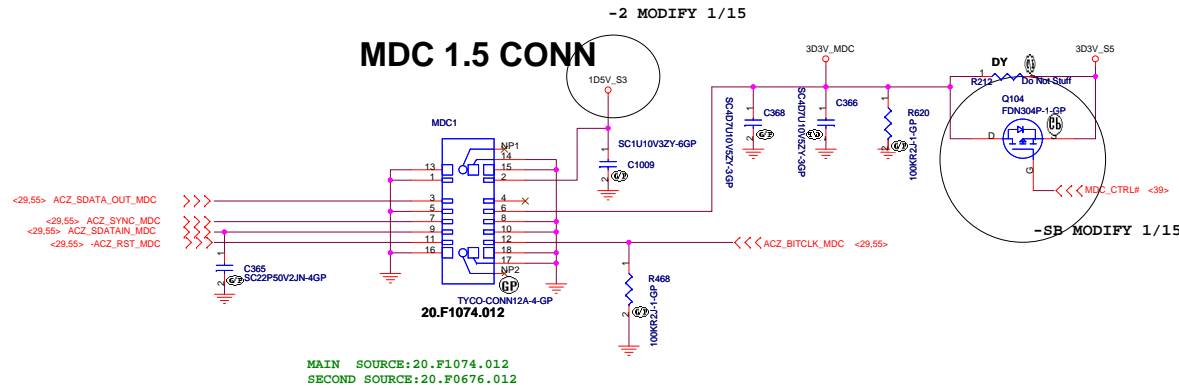


MAIN SOURCE:20.F0772.008
SECOND SOURCE:20.F0983.008



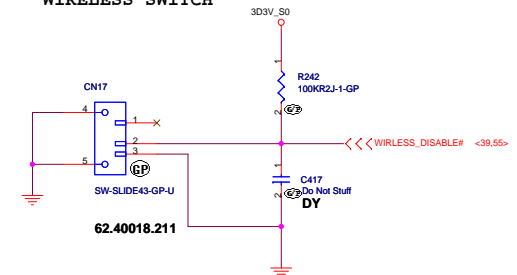
CIR

MDC 1.5 CONN



MAIN SOURCE:20.F1074.012
SECOND SOURCE:20.F0676.012

WIRELESS SWITCH

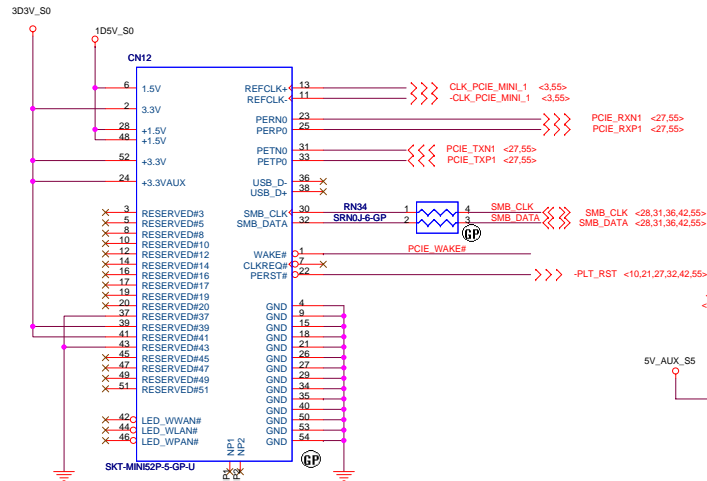


Mini PCI-E Connector

Only port-1 support USB

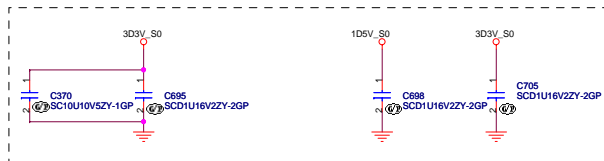
For Robson

Port-1 High



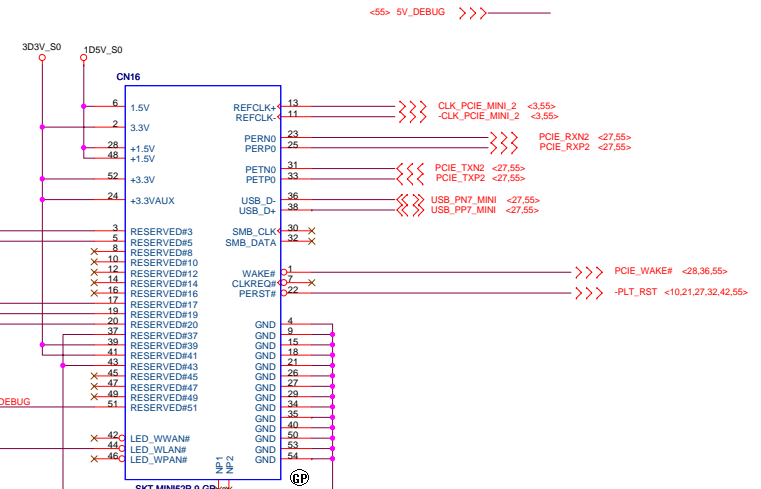
20.F0832.052

MAIN SOURCE: 20.F0832.052
SECOND SOURCE: 20.F1107.052



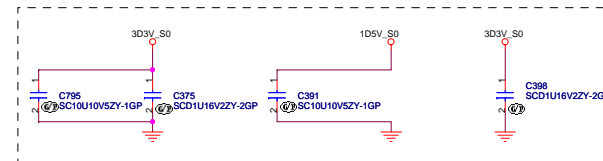
Mini PCI-E Connector

Port-2 low



62.10043.411

MAIN SOURCE: 62.10043.411
SECOND SOURCE: 20.F1084.052



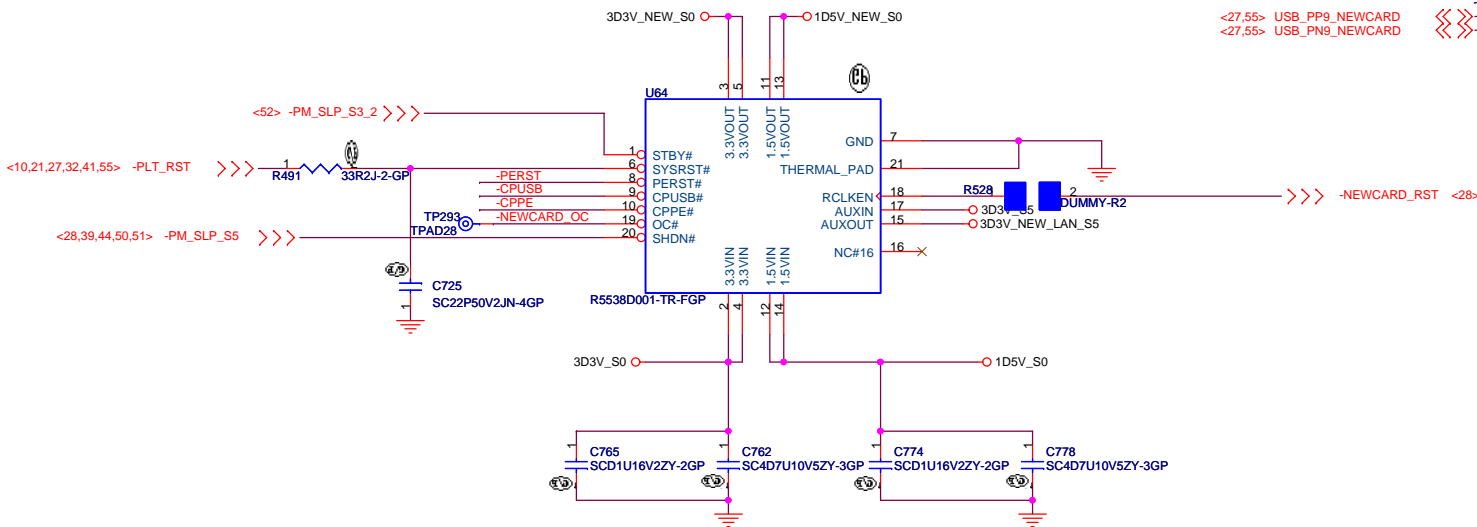
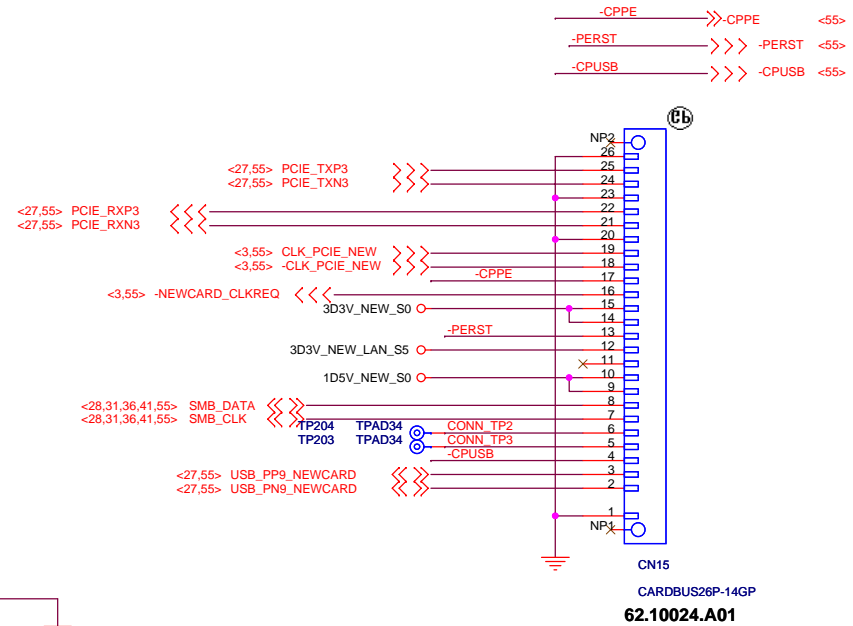
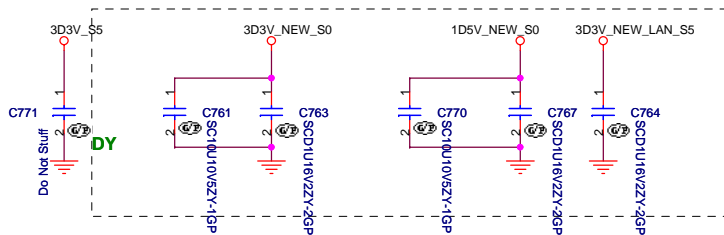
BOM1

NEWCARD Connector

For Newcard socket

Place them Near to Chip

Place them Near to Connector

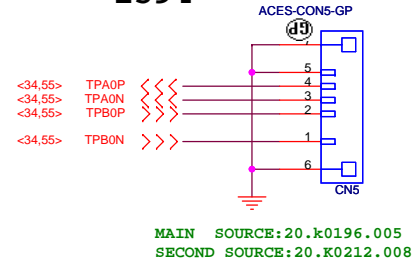


BOM1

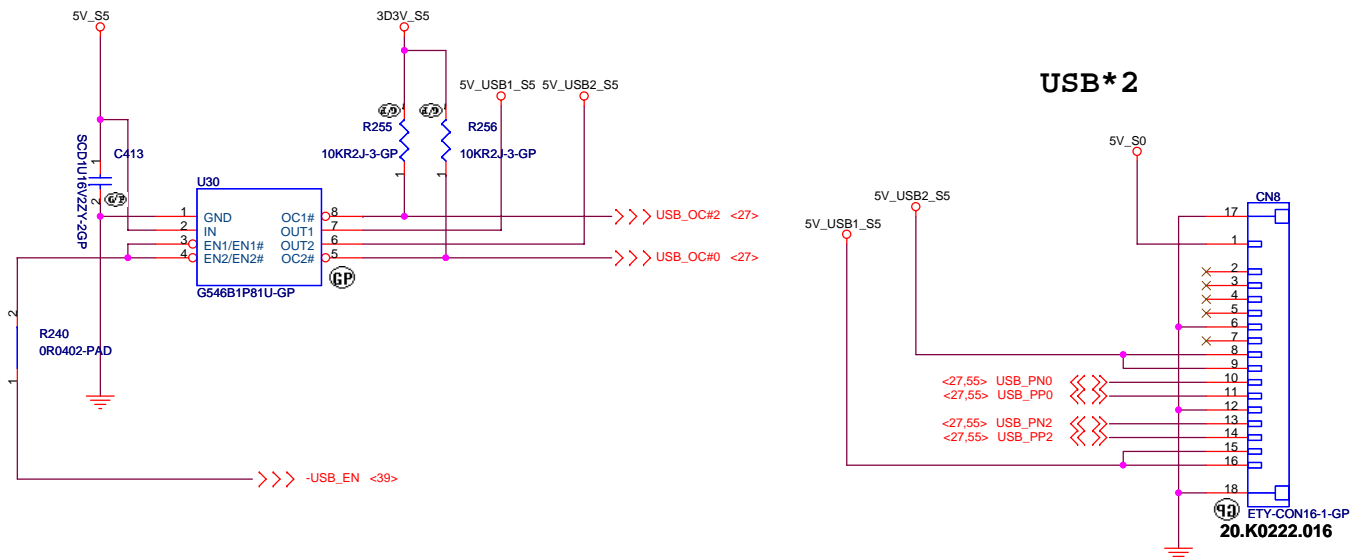
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Size	
Document Number	
Date: Monday, July 07, 2008	
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Low -End USB BOARD

1394



USB*2

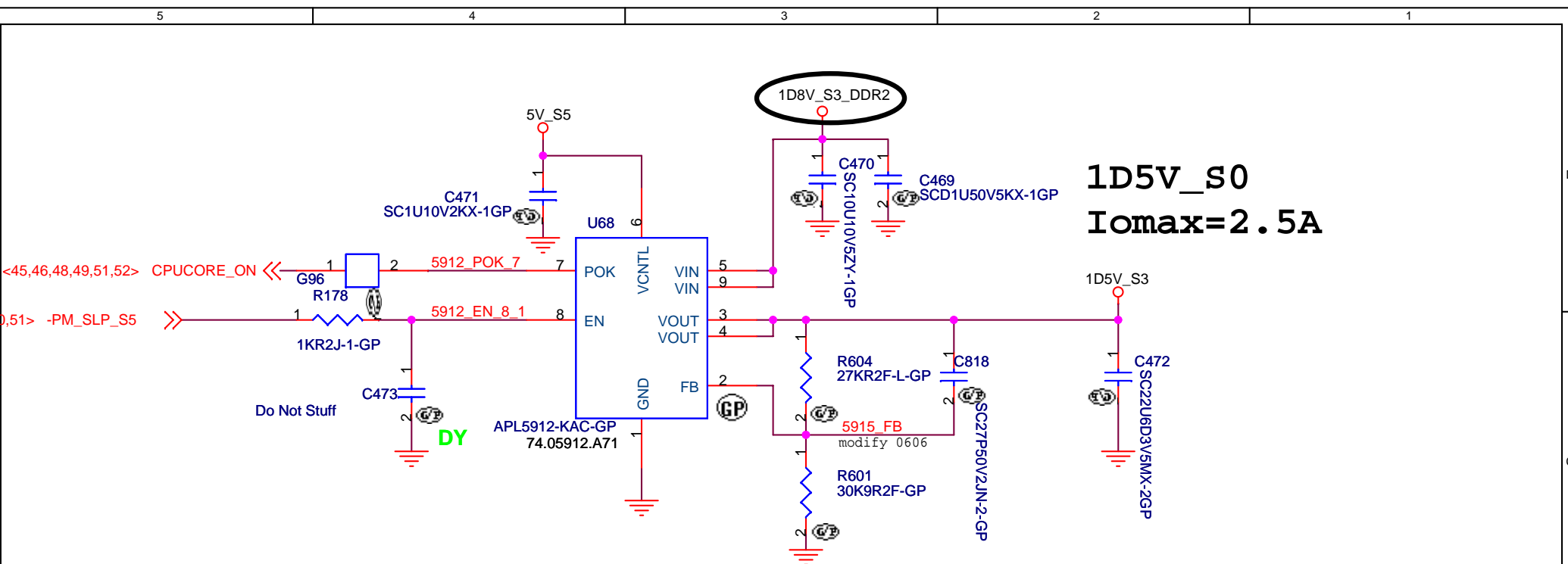


BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
USB I/O & 1394 CNN			
Size B	Document Number		Rev
	LT32M		-3
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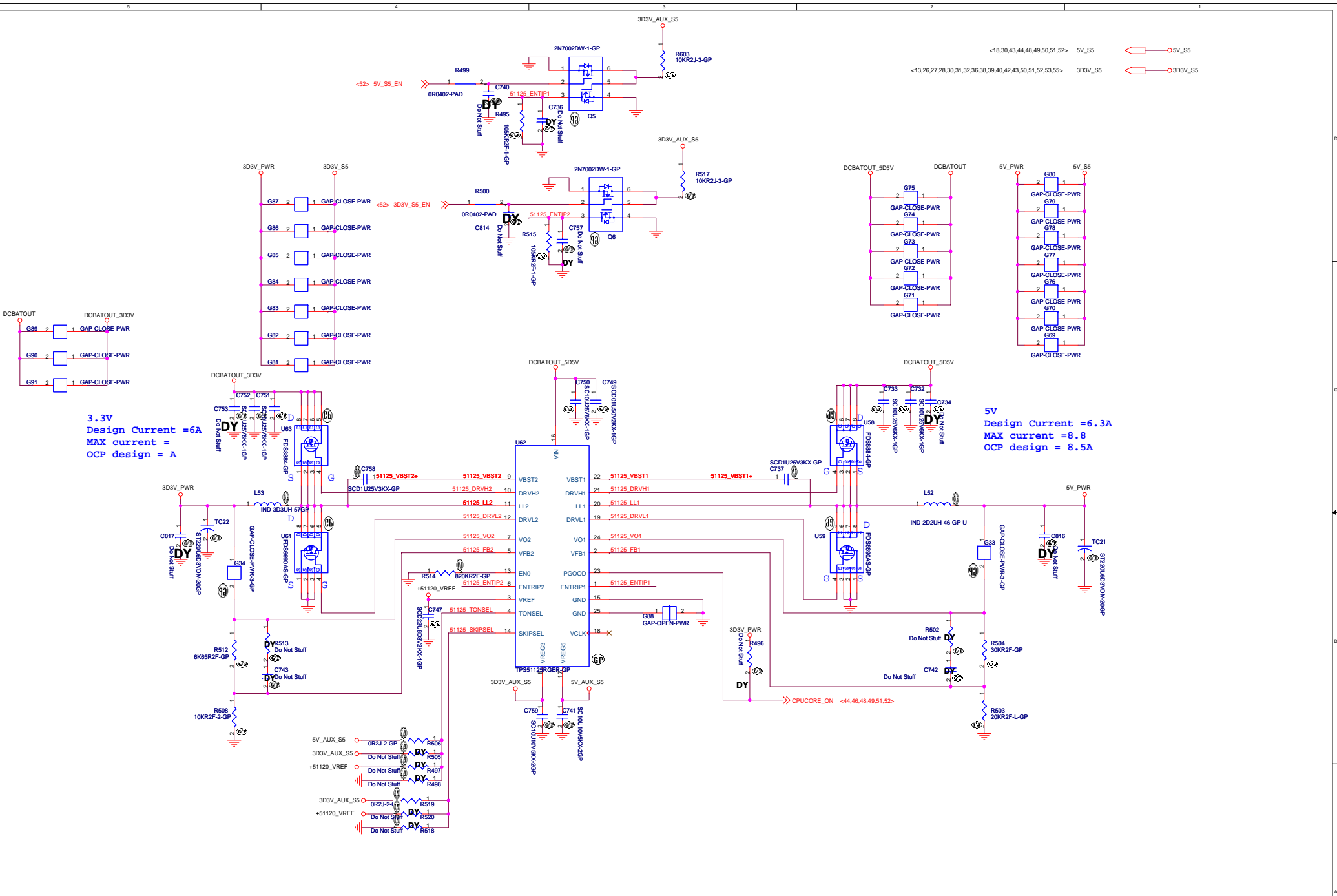
D
C
B
A



$$V_o = 0.8 * (1 + (R1 / R2))$$

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	1D5V_S0
Size	Document Number
Date: Monday, July 07, 2008 <div>Olympus</div>	
Rev	-3
Sheet	44 of 55



-SC MODIFY 1/15

<10.28> PM DPRSLPVR
<4.10.28> -DPRSTP
<10.28> -VGAET_PWVRG

-1 MODIFY

-1 MODIFY

-1 MODIFY

-1 MODIFY

sc-modify

Iomax: 38A

CPU noise

Place close to 1st phase choke

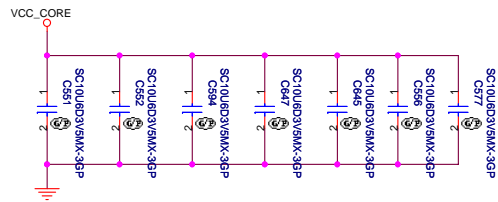
Place close to 1st Choke

<5.47> VCC_CORE

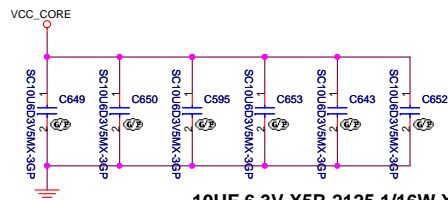
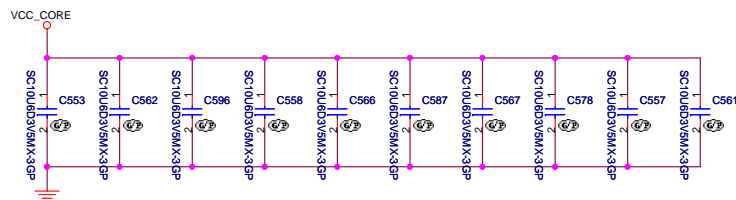
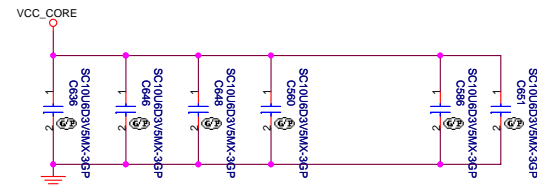
BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taipai Hsien 221, Taiwan, R.O.C.

File: ISL6266A_CPU_CORE
Size: Document Number: LT32M
Date: Monday, July 07, 2008 Sheet: 46 of 55



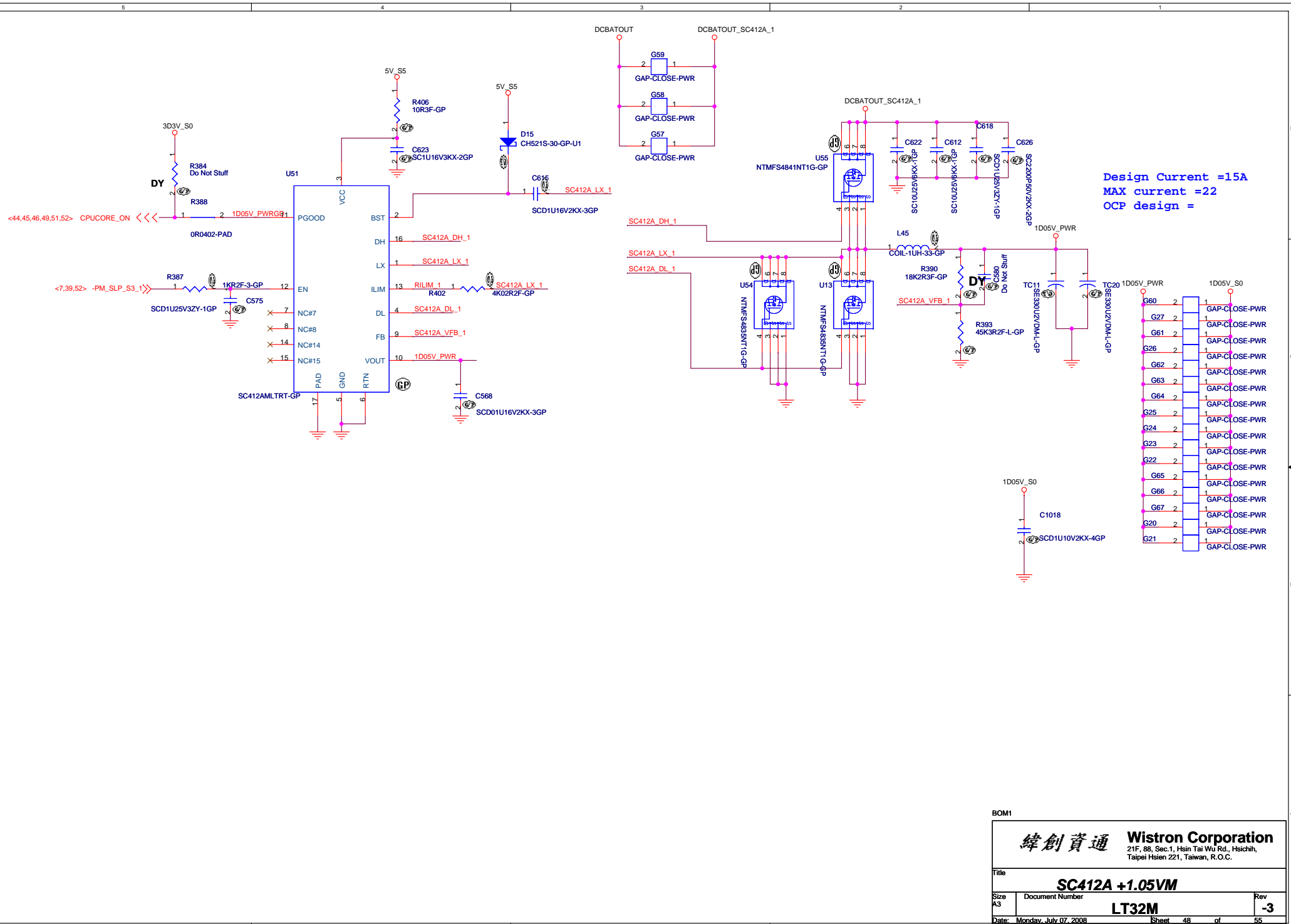
10UF 6.3V X5R 2125 1/16W X16 PCS



10UF 6.3V X5R 2125 1/16W X16 PCS

BOM1

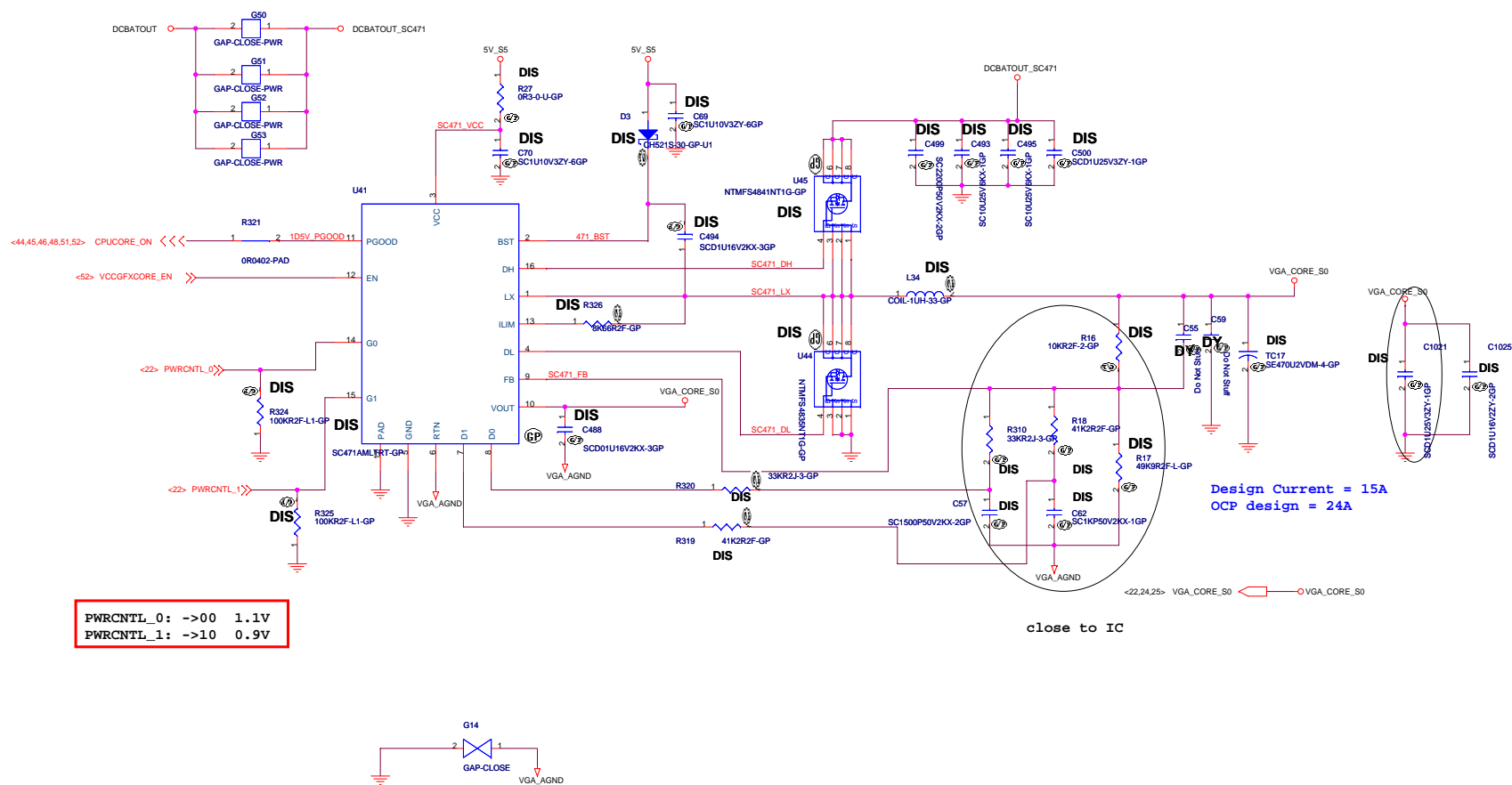
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title		VCCCPUCORE DECOUPLING	
Size Custom	Document Number LT32M	Rev -3	
Date: Monday, July 07, 2008	Sheet 47 of 55		

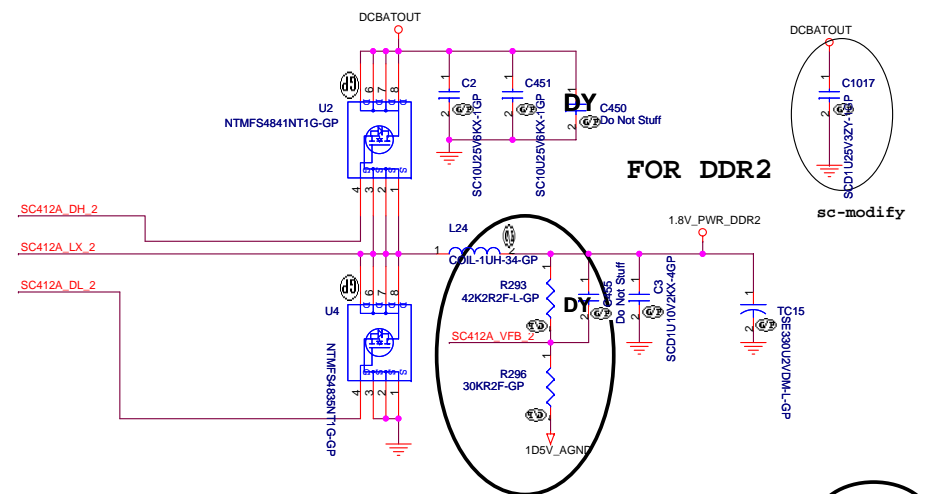


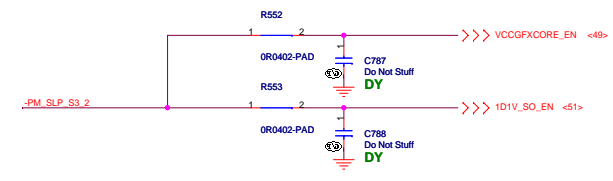
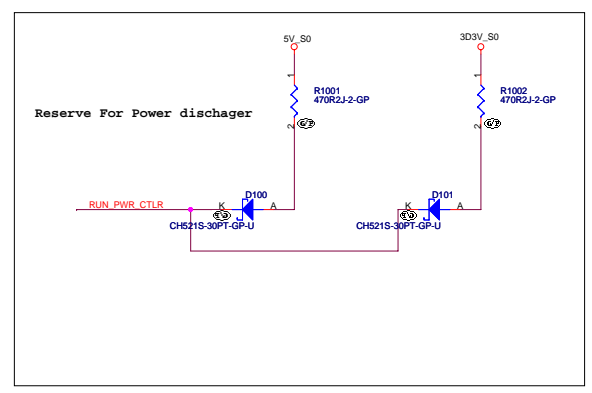
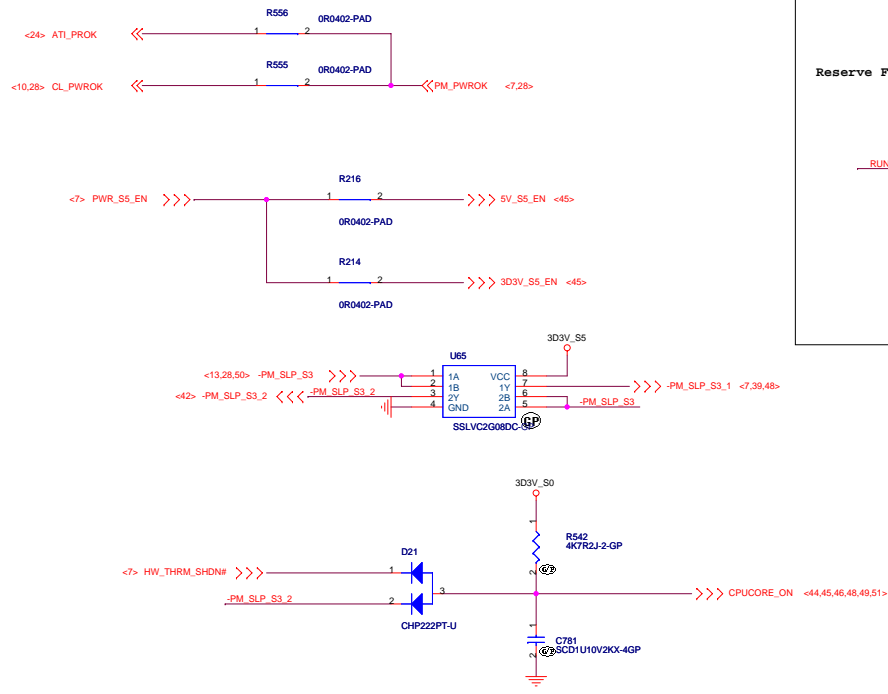
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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